

# SW6 INTEL OPTIMUS SYSTEM DIAGRAM

**+3V/+5V**  
PG.33

**+1.05V/+1.8V**  
PG.38

**CPU Core**  
PG.34

**VGA Core**  
PG.35

**+1.5VSUS**  
PG.36

**+1.05VTT**  
PG.40

**UMA VGACORE**  
PG.41

**Charger**  
PG.37

**SODIMM1**  
Max. 4GB  
PG.12

1066/1333MHZ  
DDR3  
Channel A

**SODIMM2**  
Max. 4GB  
PG.13

1066/1333MHZ  
DDR3  
Channel B

**INTEL Arrandale**  
37.5mm X 37.5mm  
989pin PGA  
TDP 35W  
PG.3~6

FDI DMI

**N11M**  
23mm X 23mm  
TDP 13~14W  
PG.14~19

**VRAM**  
128Mx16x4,64bit  
PG.18

14.318MHz  
**CLOCK GEN**  
PG.2

**HDD**  
PG.23

SATA0

**ODD**  
PG.23

SATA1

**INTEL PCH Ibex Peak-m**  
27mm X 25mm  
1071pin FCBGA  
TDP 3.5W  
PG.7~11

HDMI  
CRT

HDMI  
Level  
Shifter

**HDMI**  
PG.21

**CRT**  
PG.22

LVDS

**LVDS**  
PG.20

**USB2.0 Ports X3**  
PG.28

**Webcam**  
PG.20

USB 2.0

PORT0,1

PORT2

PORT4

**Card Reader**  
RTS5159  
PG.24

**Stackup**  
TOP  
GND  
IN1  
IN2  
VCC  
BOT

**PCI-E x 1**  
LANE1 LANE0  
**LAN**  
RTL8103EL-VB-GR  
10/100  
PG.27  
**WLAN BT COMBO**  
PG.32  
**USB 2.0**  
PORT10

**KBC**  
EnE KB3926QF D2  
PG.30  
KB 29 TP 29 ROM FAN PG.23

**HP/MIC**  
PG.25


**Digital MIC**  
PG.25

Azalia

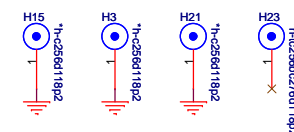
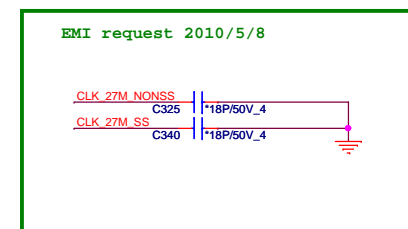
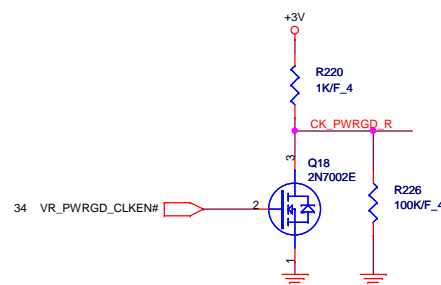
**AUDIO CODEC**  
ALC272  
PG.25

**AMP**  
TPA6017  
PG.26

**Speaker**  
PG.26

  
**Quanta Computer Inc.**  
PROJECT : SW6  
Block Diagram  
Date: Tuesday, May 25, 2010 Sheet 1 of 42



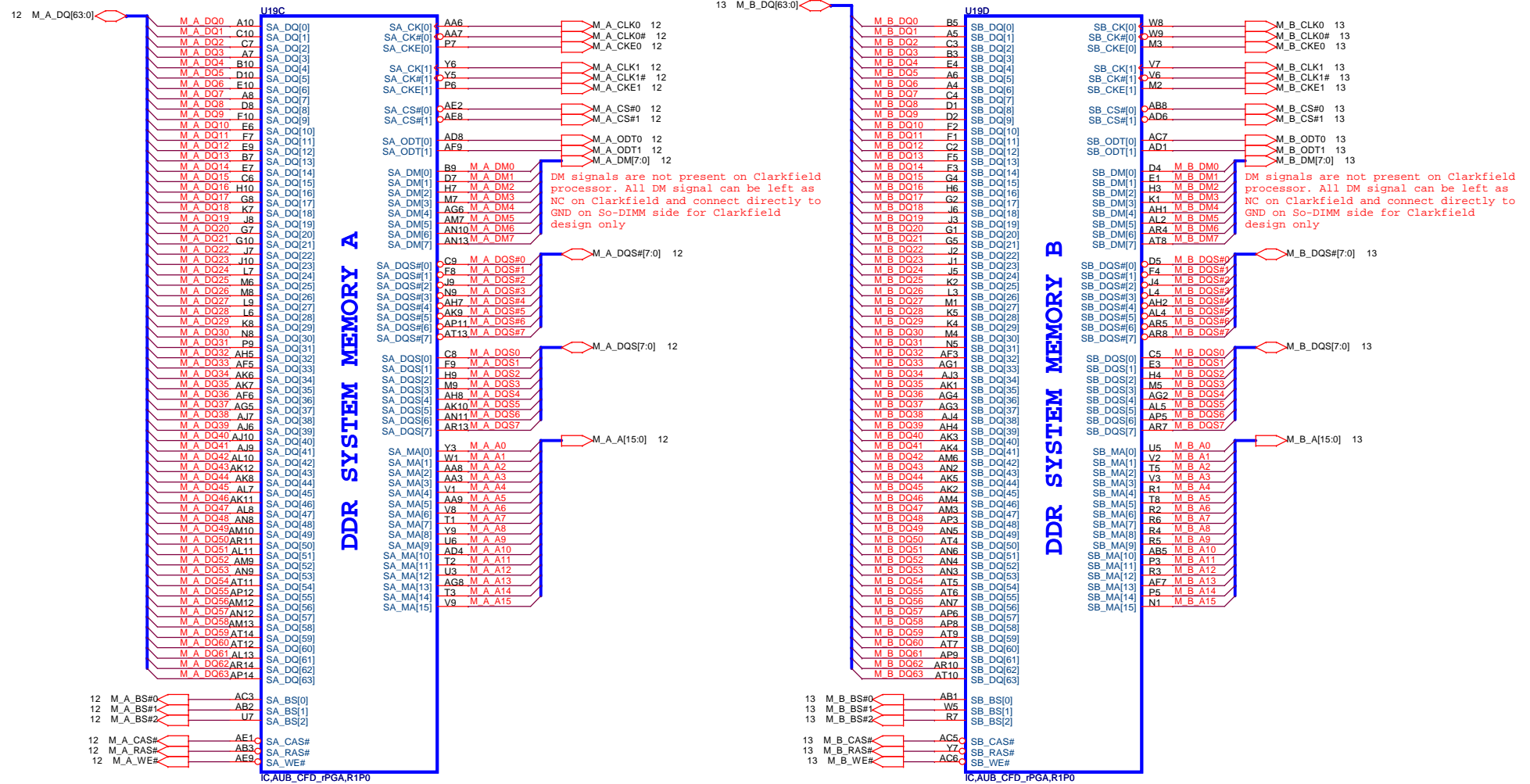




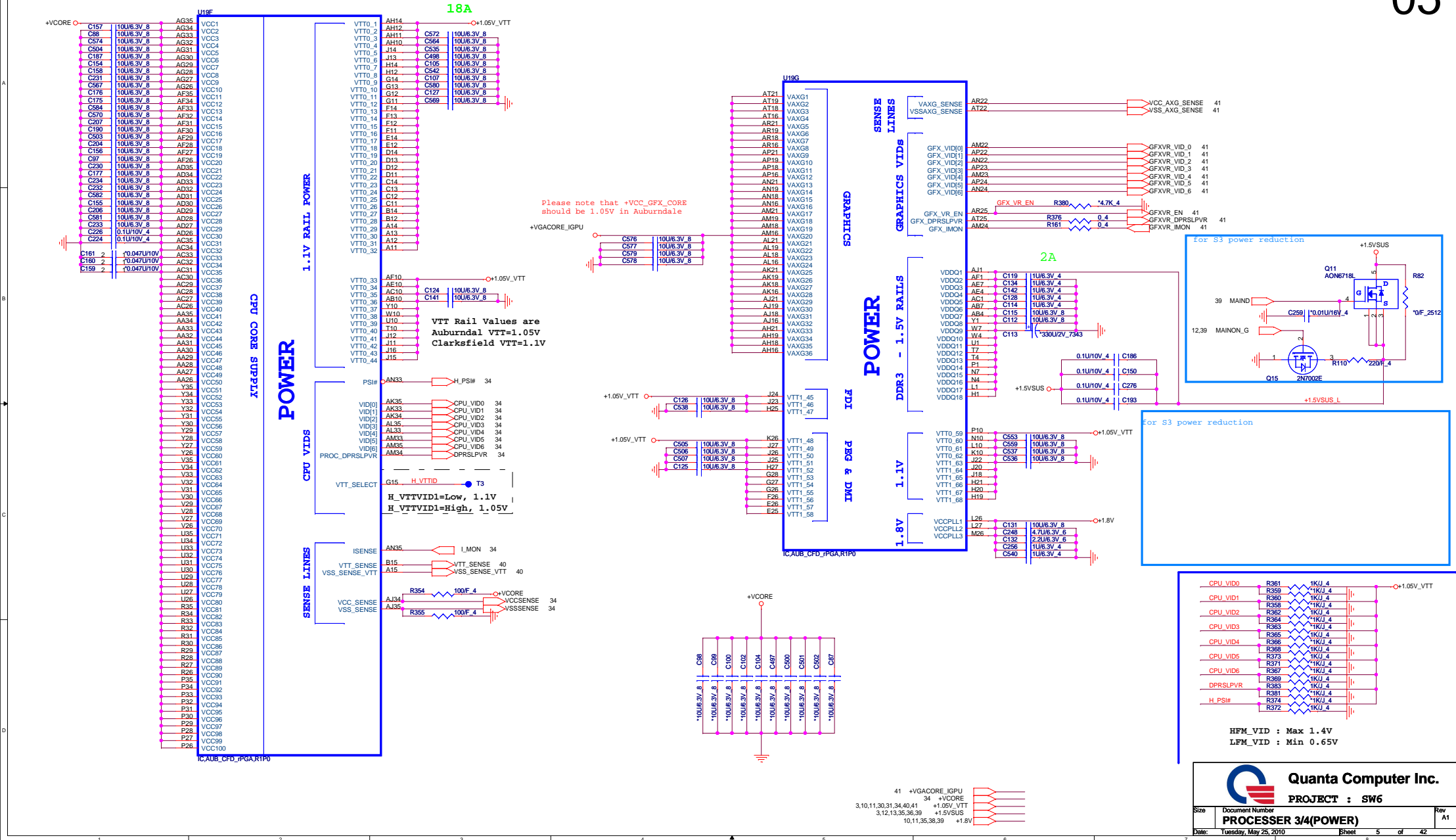




## AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



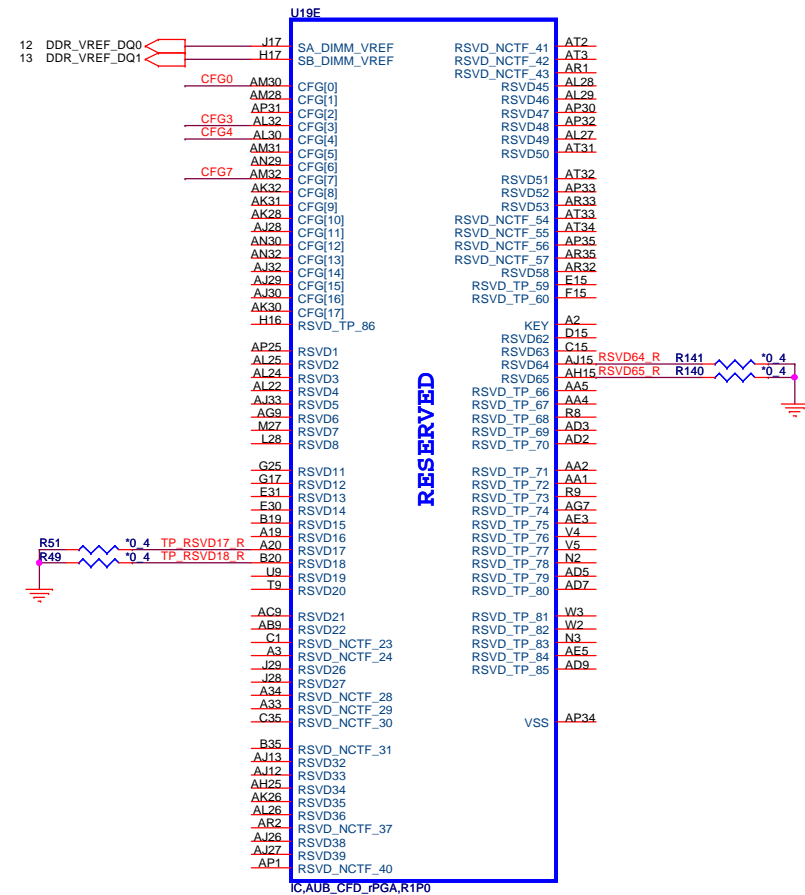
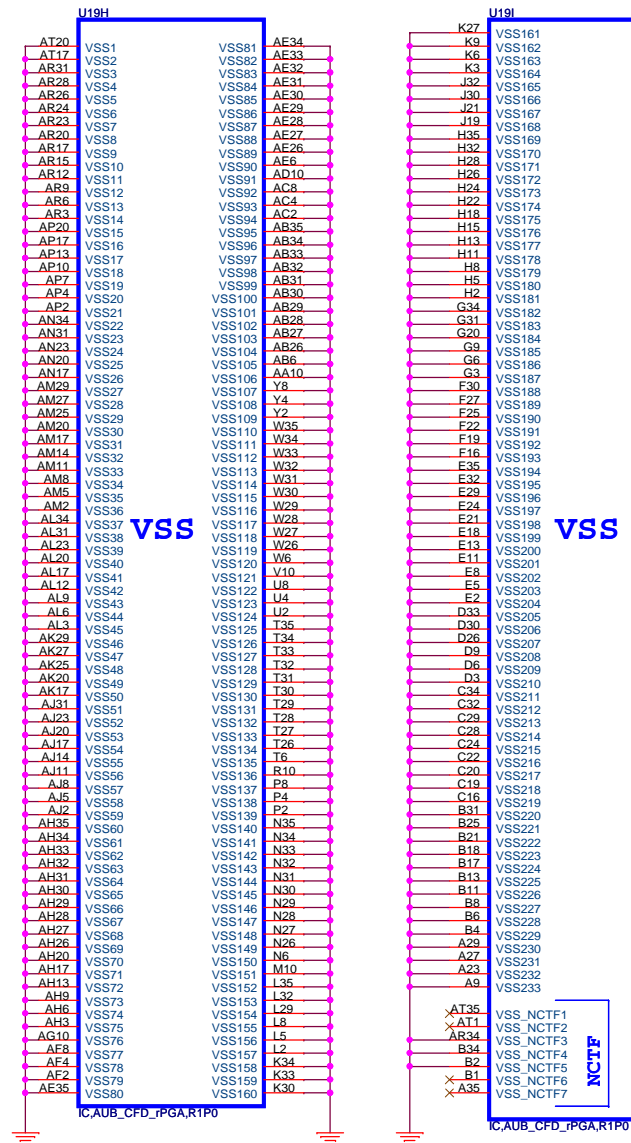






## AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

## AUBURNDALE/CLARKSFIELD PROCESSOR( RESERVED, CFG)



For Discrete only



CFG[ 1:0 ] - PCI\_Epress Configuration Select

\* 11= 1 x 16 PEG

\* 10= 2 x 8 PEG

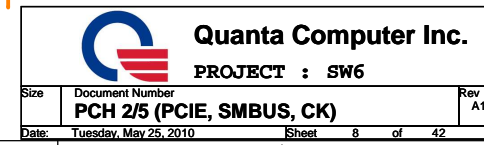
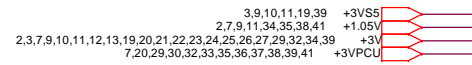
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0, 14 -> 1

The Clarkfield processor's PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.





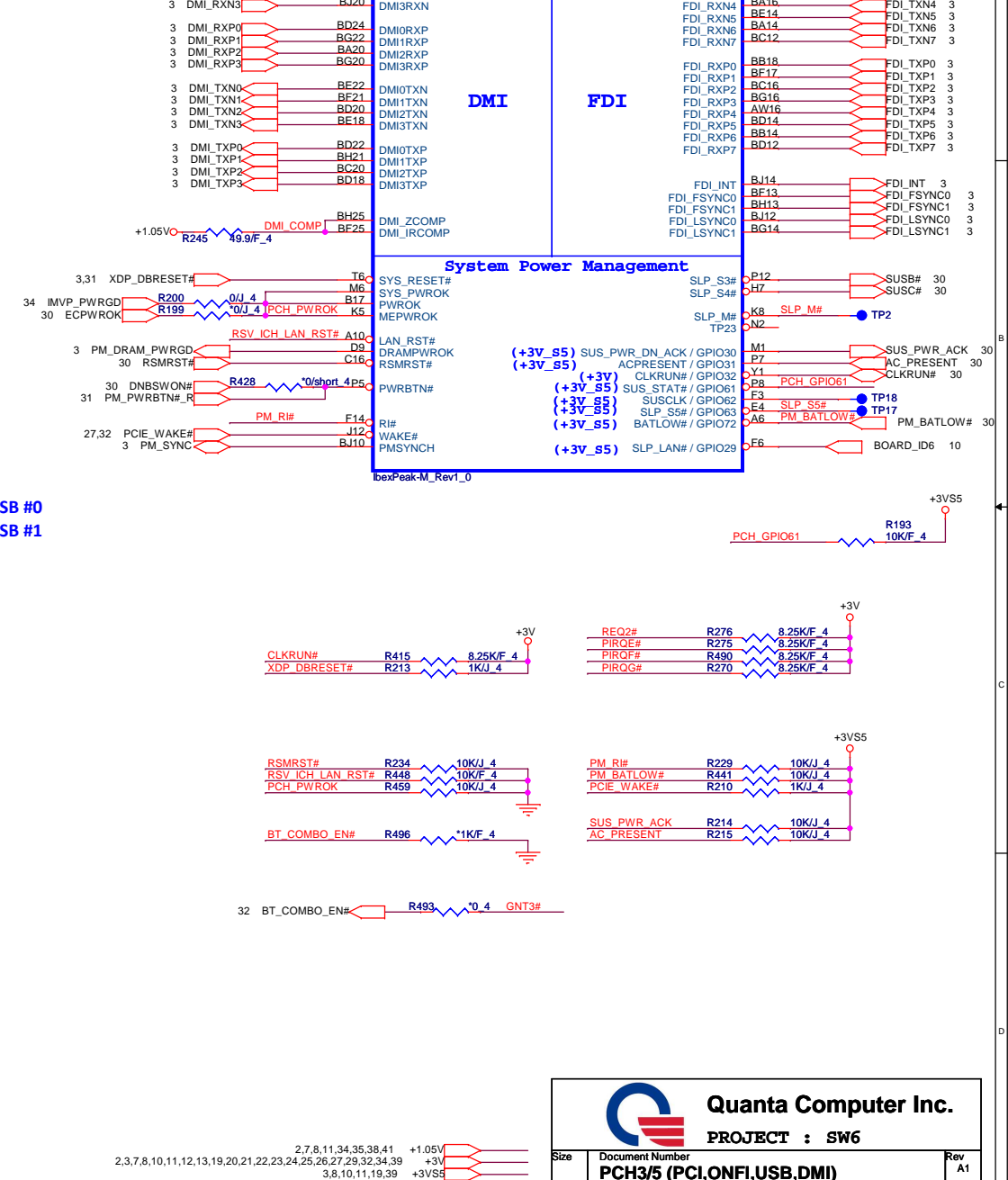






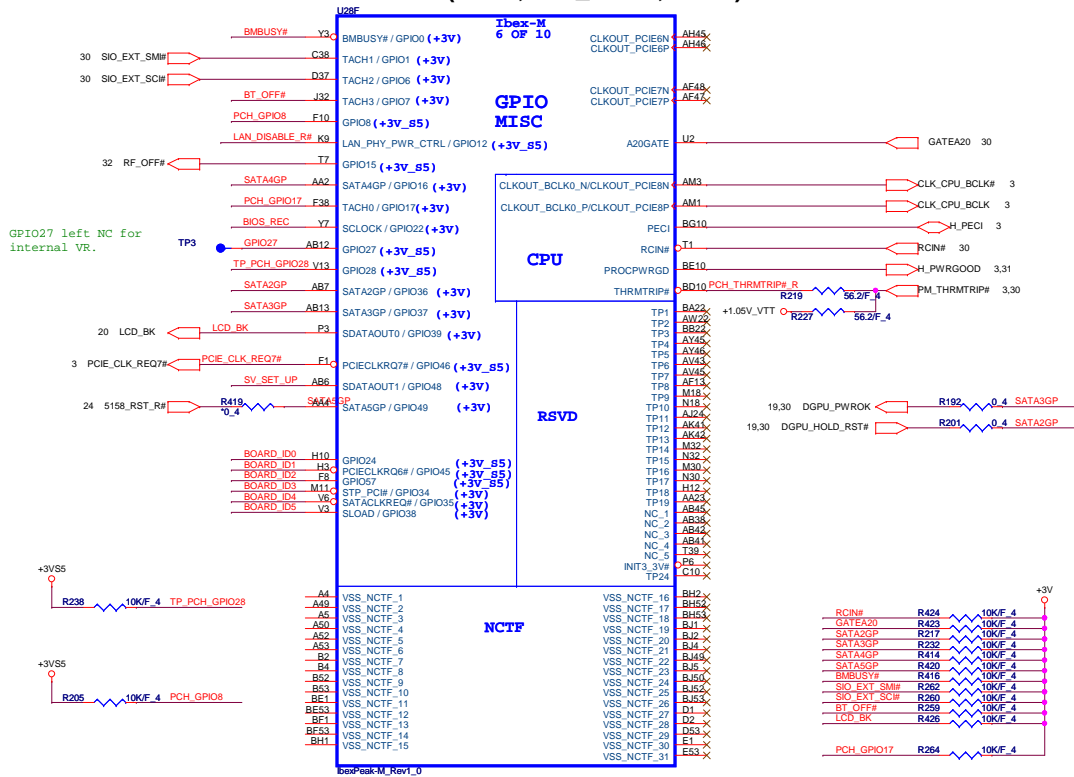
U28E

X H40	AD0	Ibex-M
X N34	AD1	5 OF 10

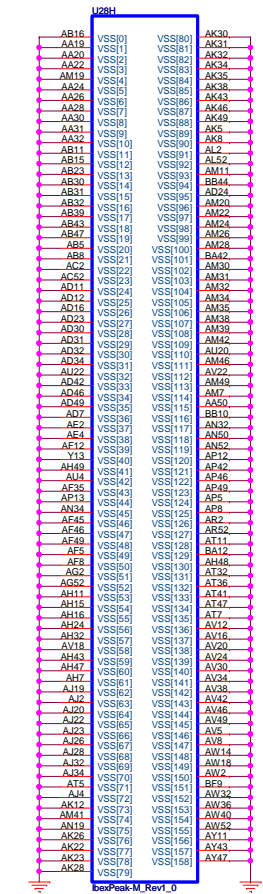




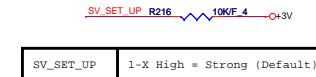
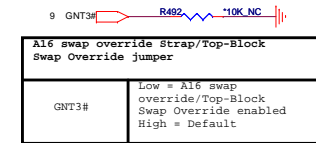
## IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)



### IBEX PEAK-M (GND)



10



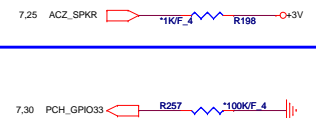
Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

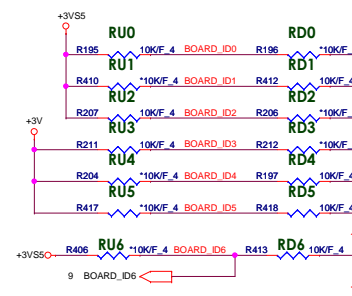
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

## No Reboot Strap

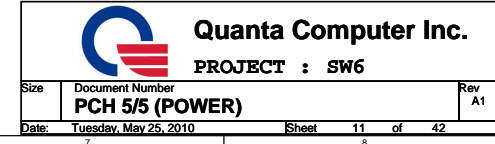
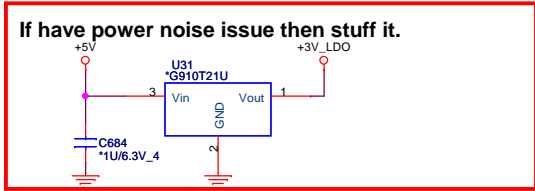


## BOARD ID SETTING

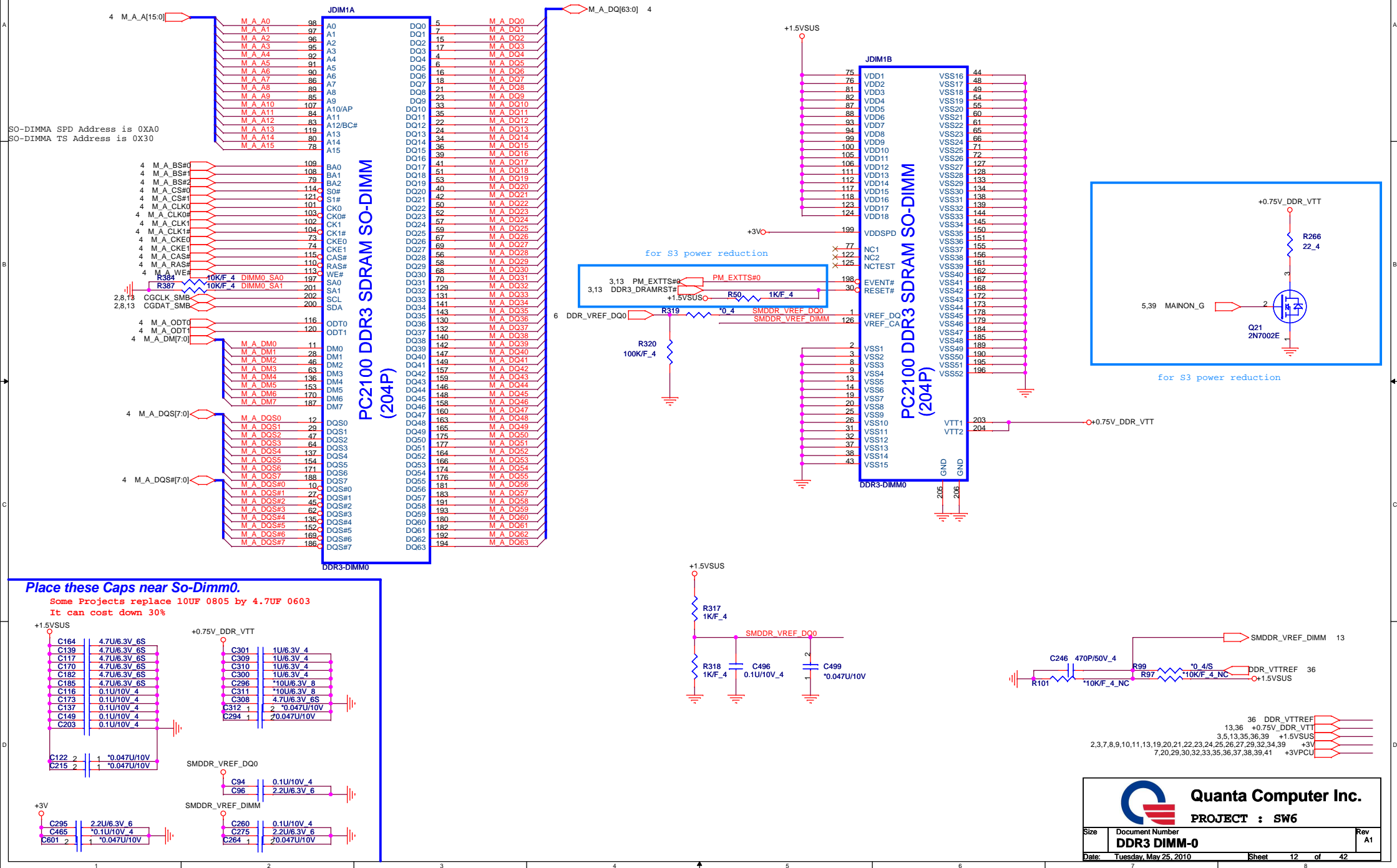
```
Board ID5: Switchable
Board ID4: Dobly
Board ID3: MDC
Board ID2: 14'' / 15.6"
Board ID1: UMA / DIS
Board ID0: LG / CB
```

[illegible]

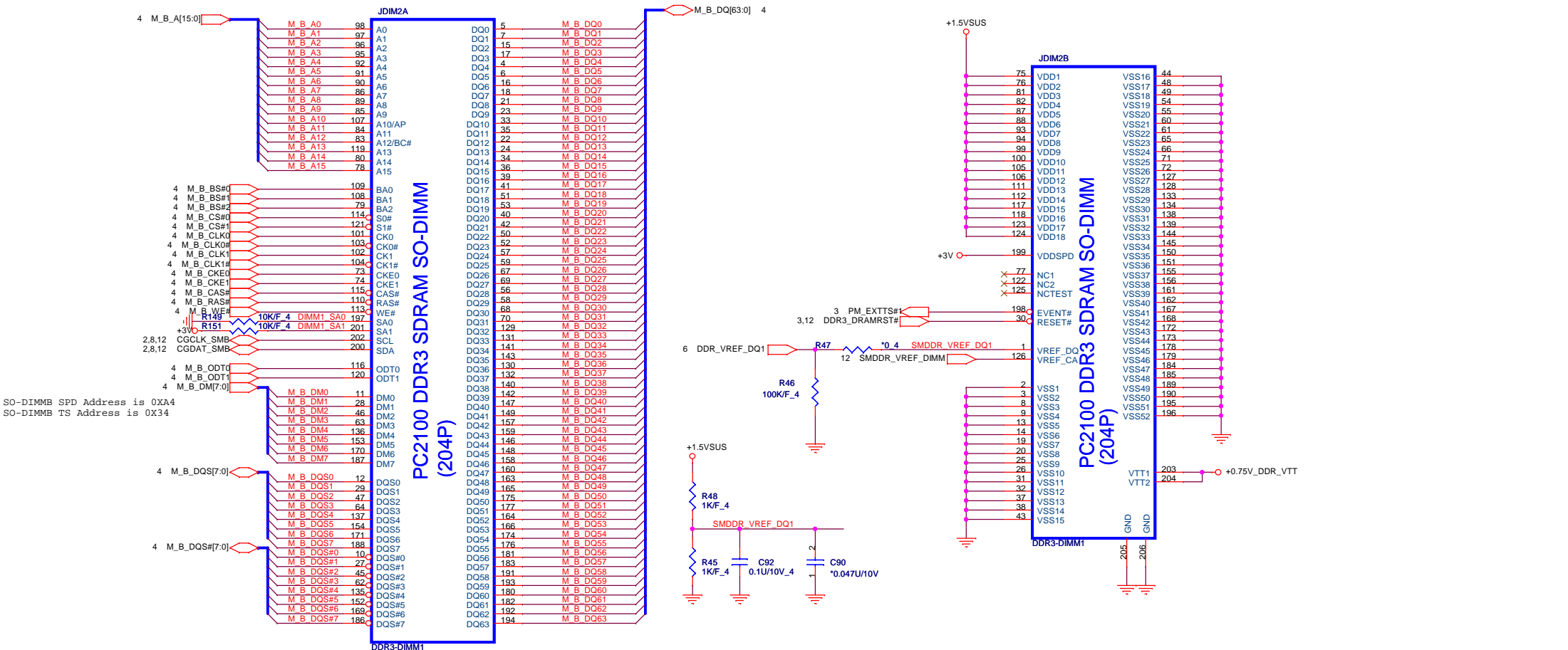




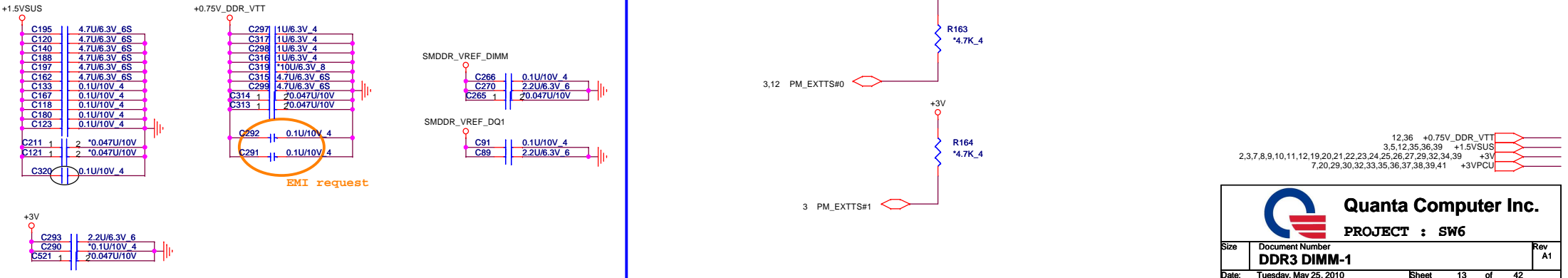






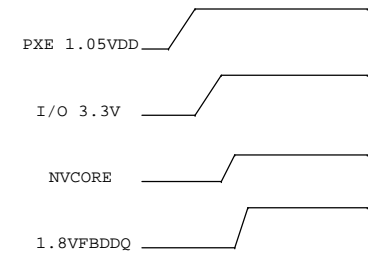


Place these Caps near So-Dimm1.  
Some Projects replace 10UF 0805 by 4.7UF 0603  
It can cost down 30%

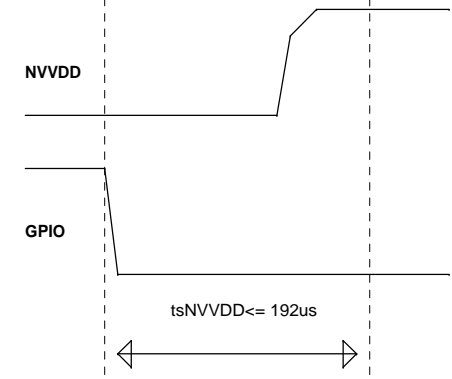




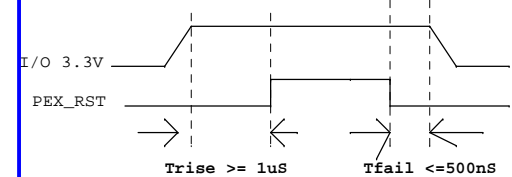
**power up sequence**



**NB9M: VGACORE +0.90V (Normal) , +1.09V**  
**NVVDD Maximum Settling Time**



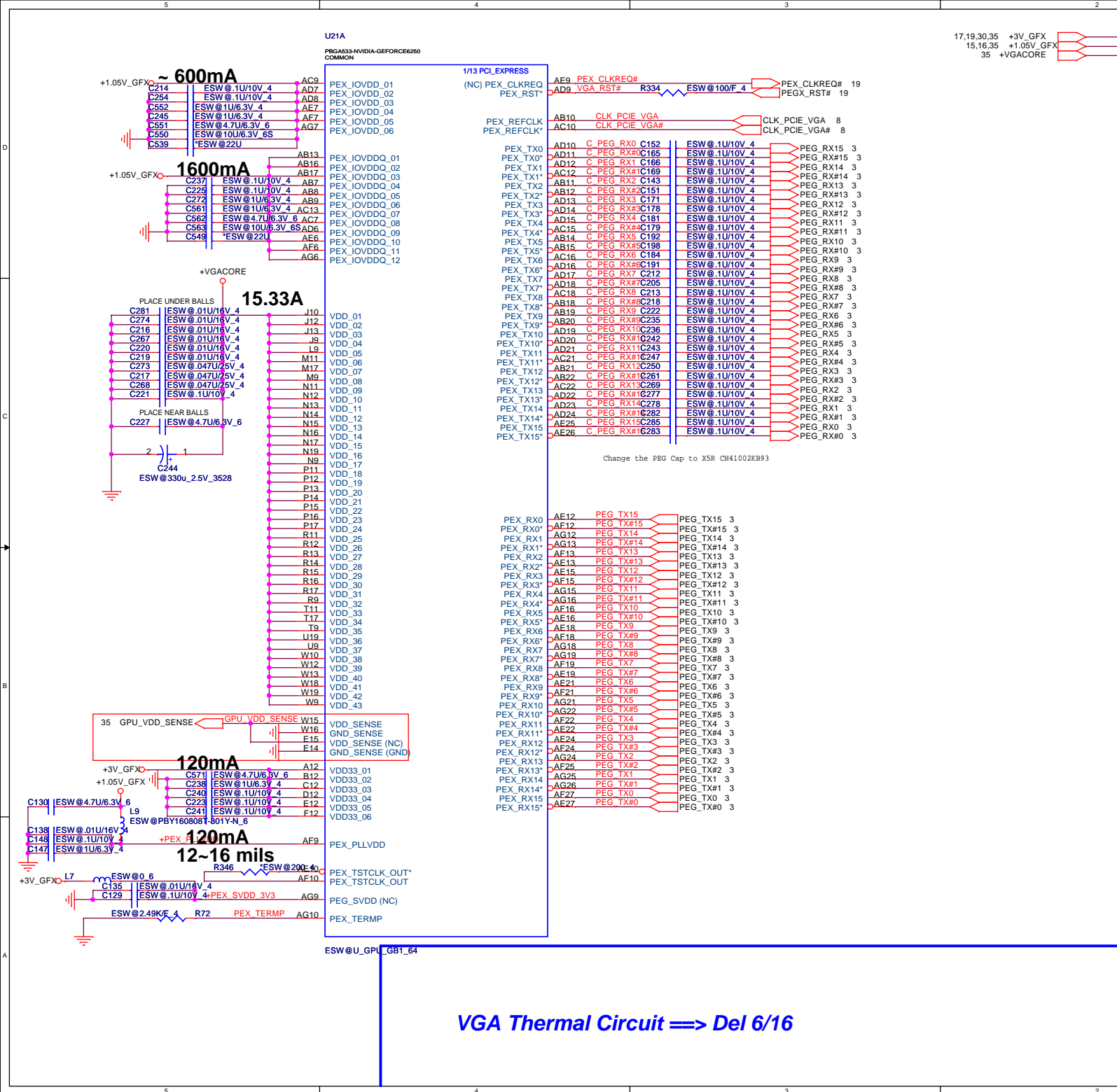
## PEX\_RST timing



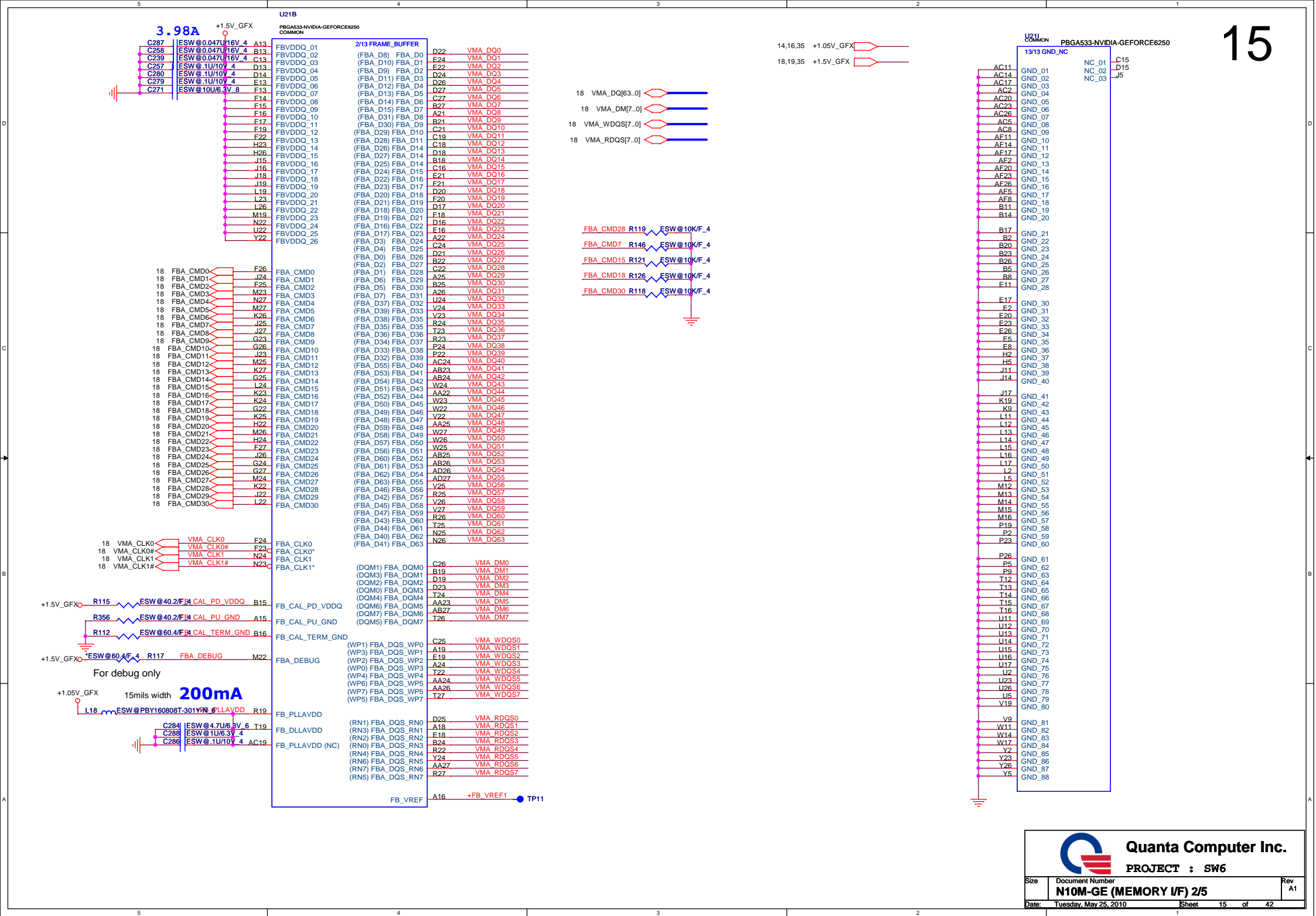
**Quanta Computer Inc.**

**PROJECT : SW6**

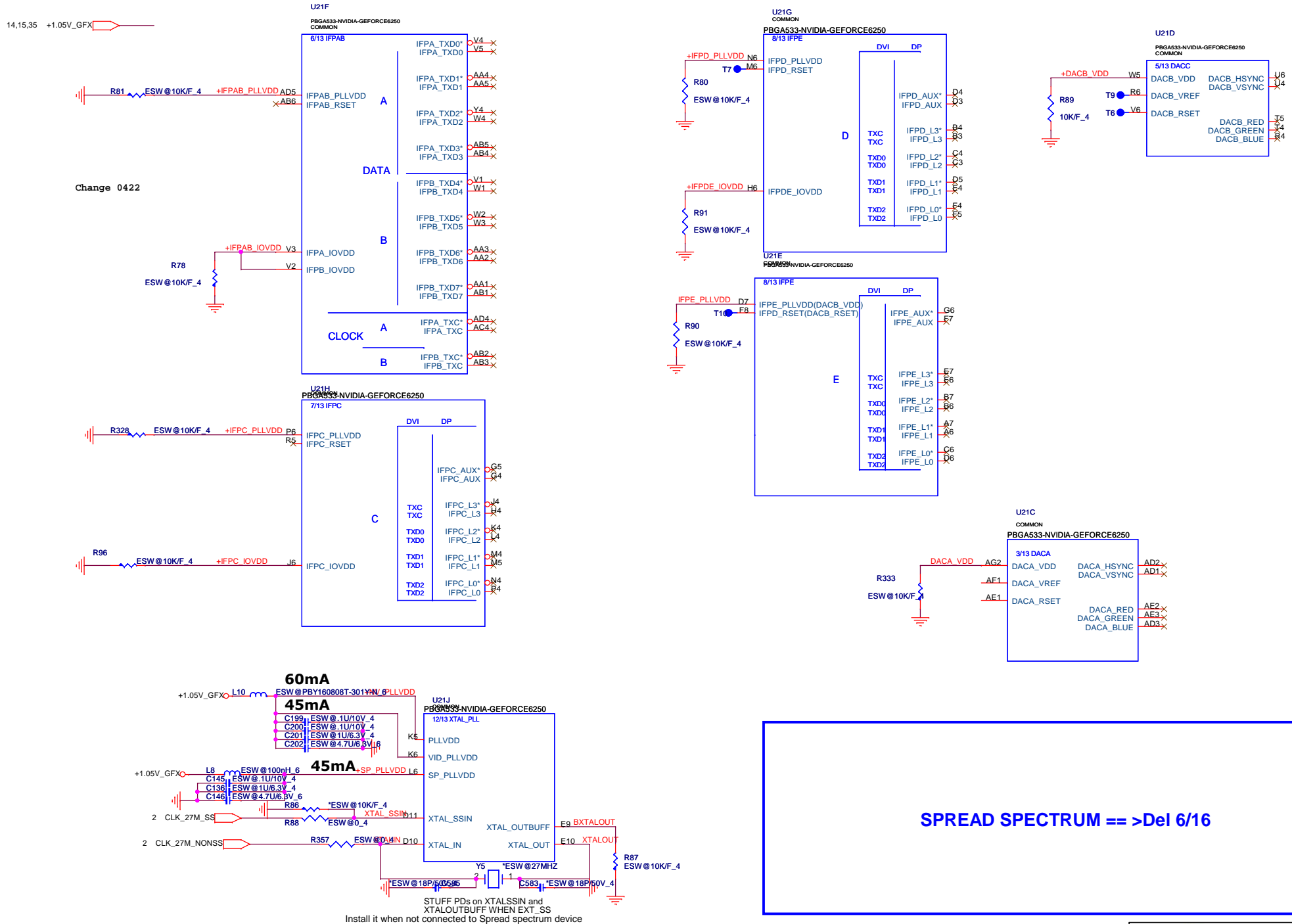
Size	Document Number <b>N10M-GE (PCIE I/F) 1/5</b>	Rev A1
Date:	Tuesday, May 25, 2010	Sheet 14 of 42





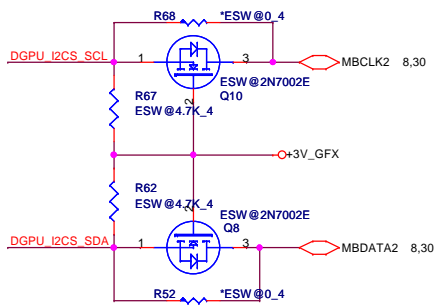
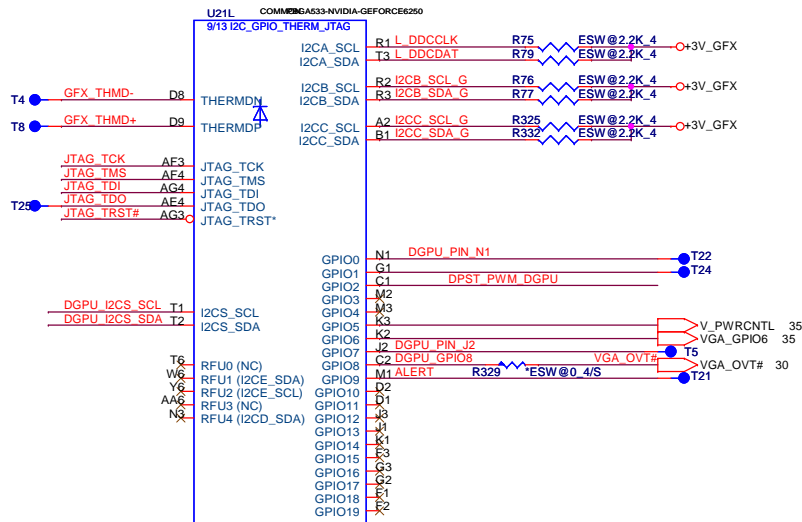
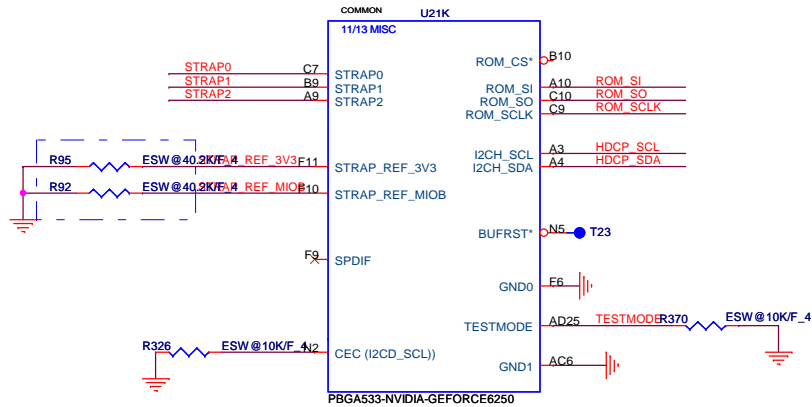






**SPREAD SPECTRUM == >Del 6/16**





Mount Q15, Q30, R801, R802  
For Switchable only

14,19,30,35 +3V\_GFX

CHIP	PCI_DEVID:	STRAP2
NB11M-GE2	0x0A70	0000 PD 5K

Logical Strap Bit Mapping		
	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1% (0402)]  
 10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]  
 15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]  
 30.1K/F 4: CS33012FB18 [RES CHIP 30.1K 1/16W +1% (0402)]  
 35.7K/F 4: CS33572FB13 [RES CHIP 35.7K 1/16W +1% (0402)]  
 45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1% (0402)]

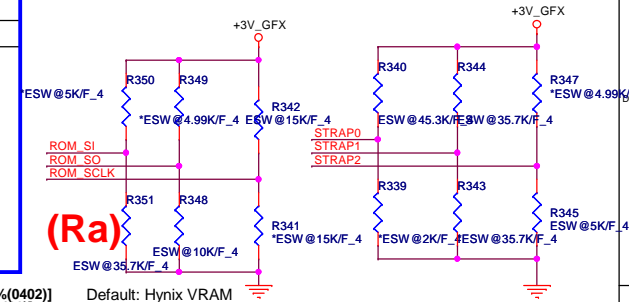
NB11M-GE2	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	1110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0110	DDR3 128Mx16x8, 64bit, 1GB,800MHz	Hynix	H5TQ2G63BFR-12C	PD 35K
0111	DDR3 128Mx16x8, 64bit, 1GB,800MHz	Samsung	K4W2G1646B-HC12	PD 45K

AKD5MGGT00  
AKD5MGGT501

PCI\_DEVID[4]/SUBVENDOR

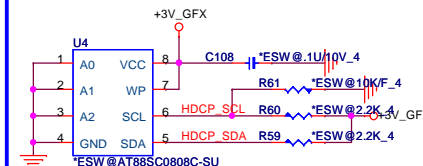


Default: Hynix VRAM

## GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVD VID0
6	OUT	N/A	NVVD VID1
7	OUT	N/A	NVVD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

## HDCP ROM



DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM



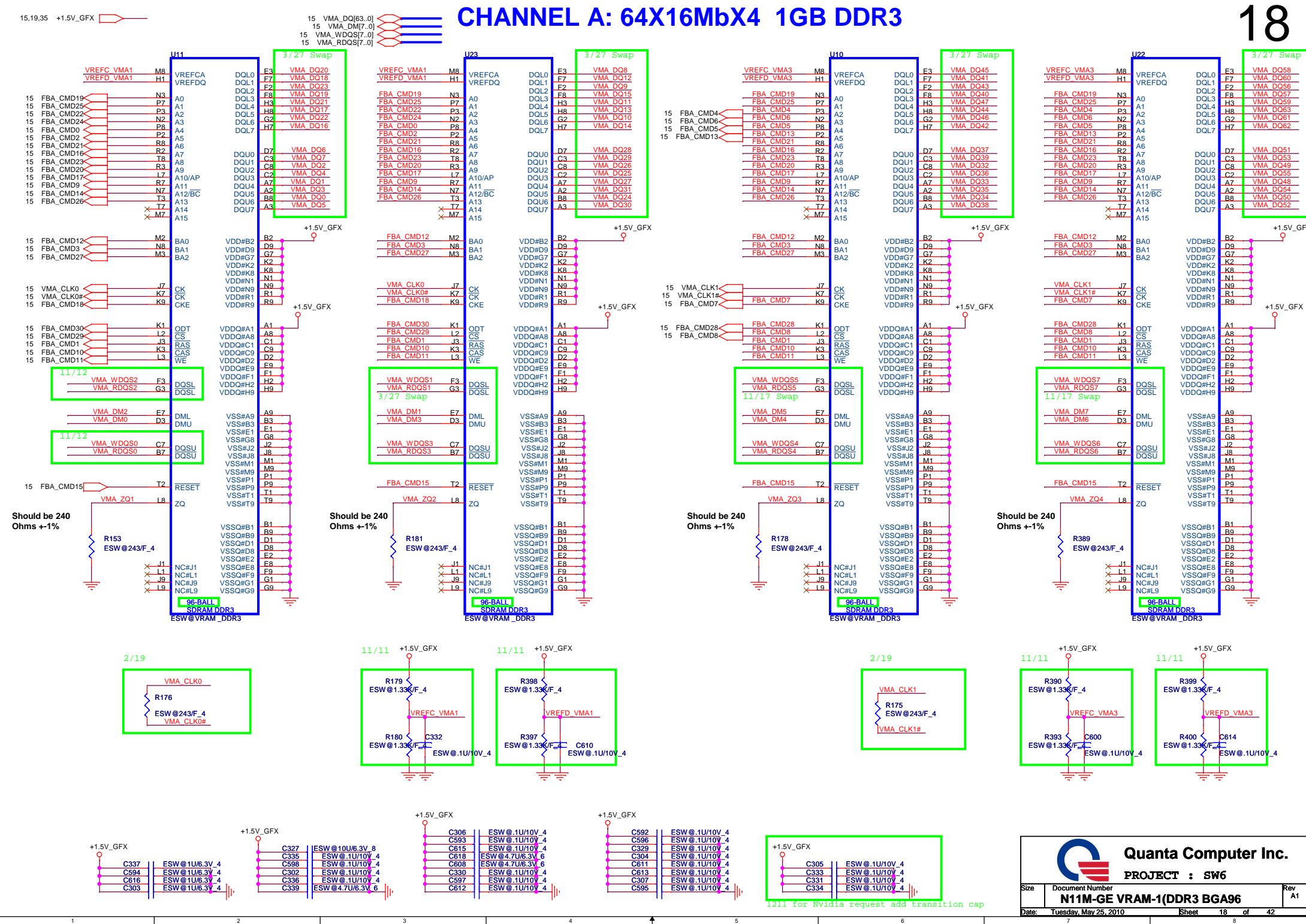
Quanta Computer Inc.  
PROJECT : SW6

Size	Document Number	Rev
	N10M-GE (GPIO&STRAPS) 4/5	A1

Date: Tuesday, May 25, 2010 Sheet 17 of 42

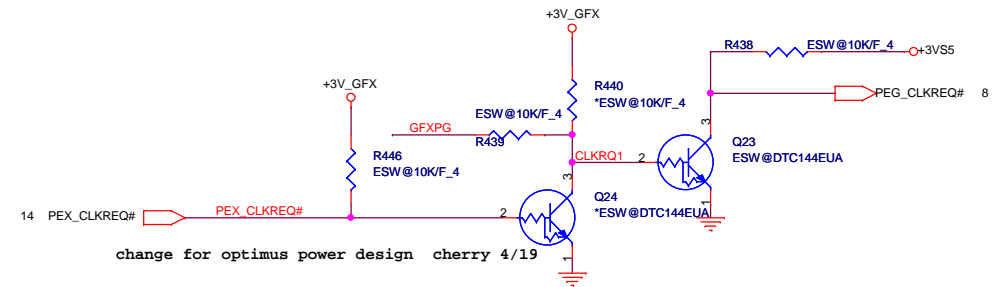
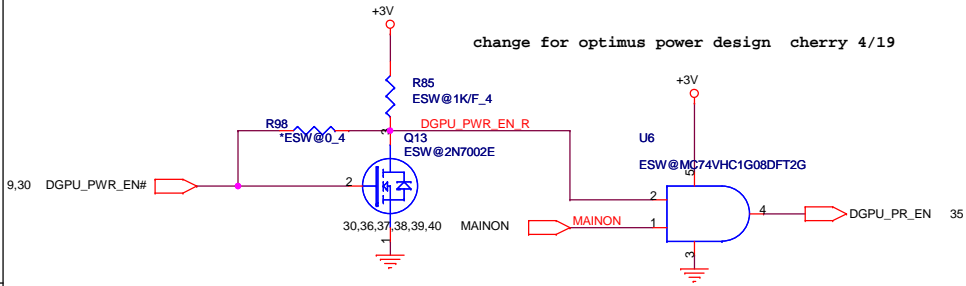


# CHANNEL A: 64X16MbX4 1GB DDR3

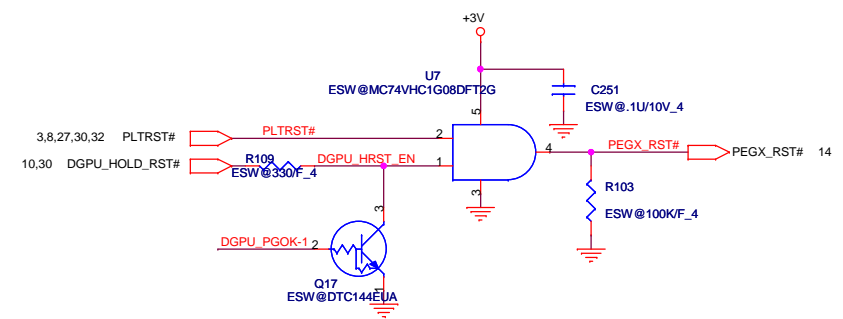
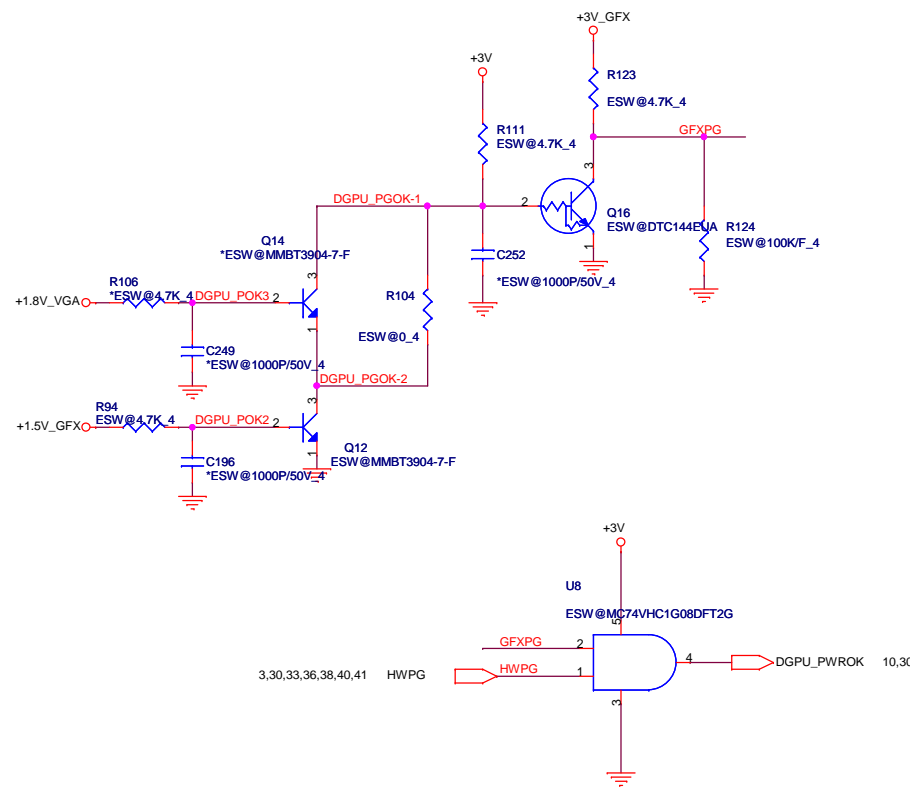




change for optimus power design cherry 4/19



change for optimus power design cherry 4/19



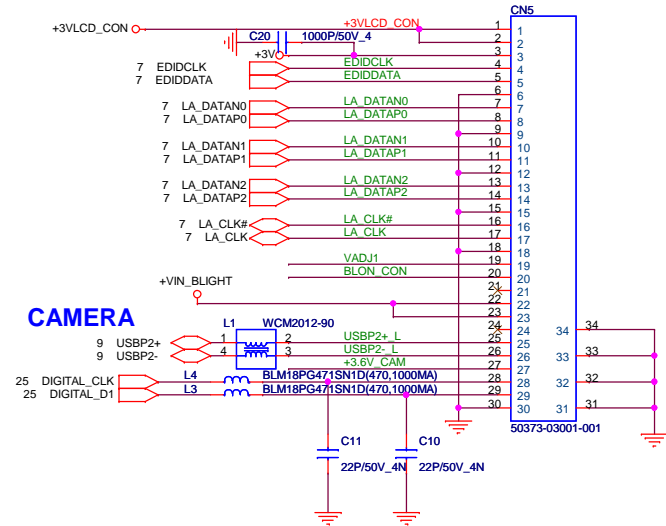
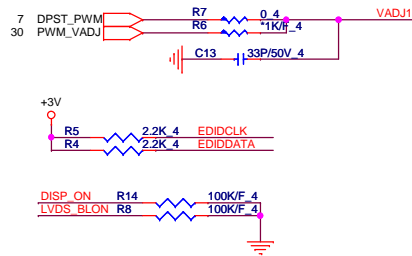
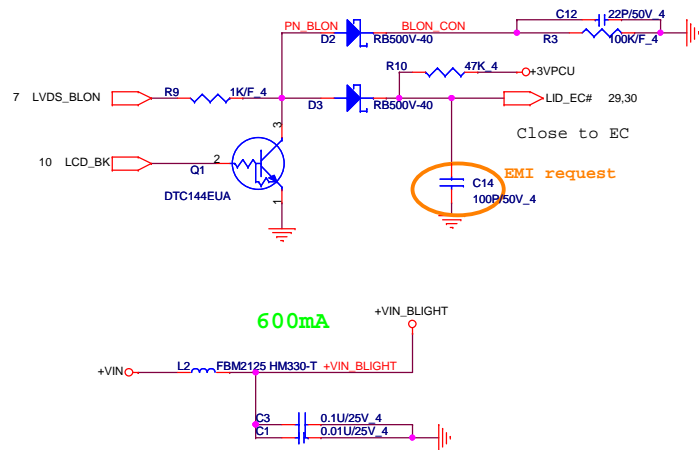
**Quanta Computer Inc.**  
 PROJECT : SW6

Size	Document Number	Rev
	Optimus power control	A1
Date:	Tuesday, May 25, 2010	Sheet 19 of 42



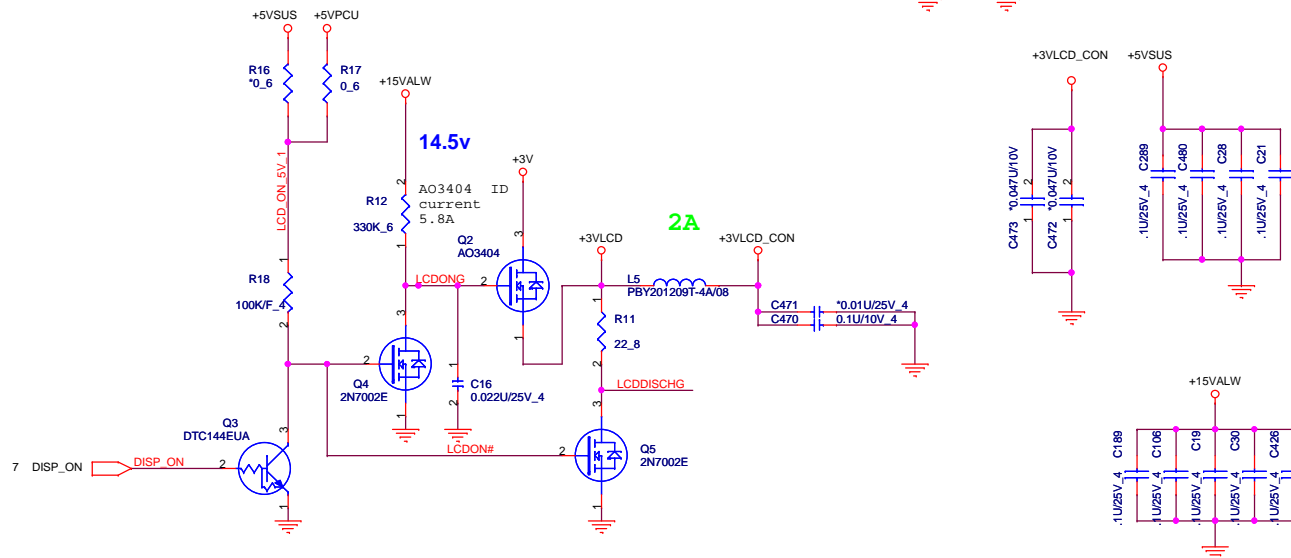
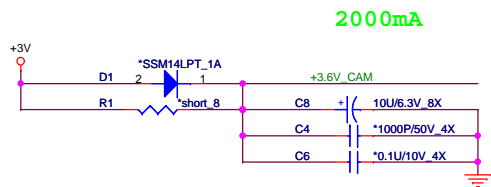
# LID Switch

20



## CAMERA

Keep same as TE2's



2,3,7,8,9,10,11,12,13,19,21,22,23,24,25,26,27,29,32,34,39  
7,29,30,32,33,35,36,37,38,39,41  
11,21,22,23,25,26,29,32,39  
29,39  
33,35,39  
33,34,35,36,37,38,39,41

+3V  
+3VPCU  
+5V  
+5VSUS  
+15VALW  
+VIN



Signals		PDT	CHR	PIM
PC1	Ra	NC	NC	NC
HDMI_CFG0	Rb	NC	NC	NC
HDMI_CFG1	Rc	4.7K	NC	NC
REXT	Rd	499	1.2K	4.7K
PC1	Re	NC	4.7K	4.7K
HDMI_OE#	Rf	NC	4.7K	NC
PC0	Rg	4.7K	4.7K	4.7K

9/16 : PIM: need use ALP411LS000 or ALP411LS004 for capella

CHR : need Na R1182, add R1027 for capella

Vendor:PDT P/N:AL008101000

Vendor:CHR P/N:AL007318002

Vendor:PIM P/N:ALP411LS004

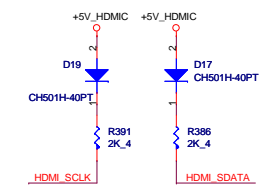
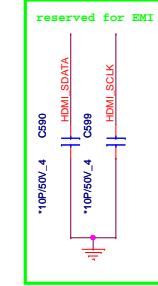
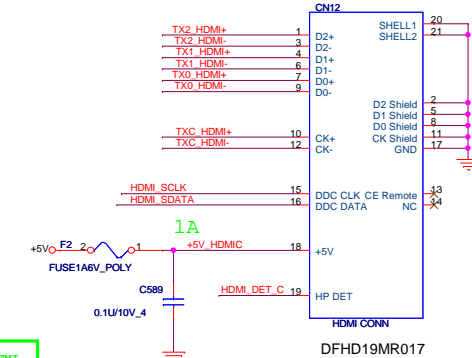
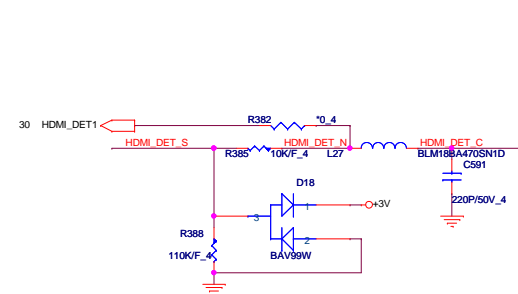
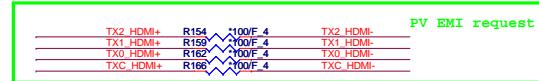
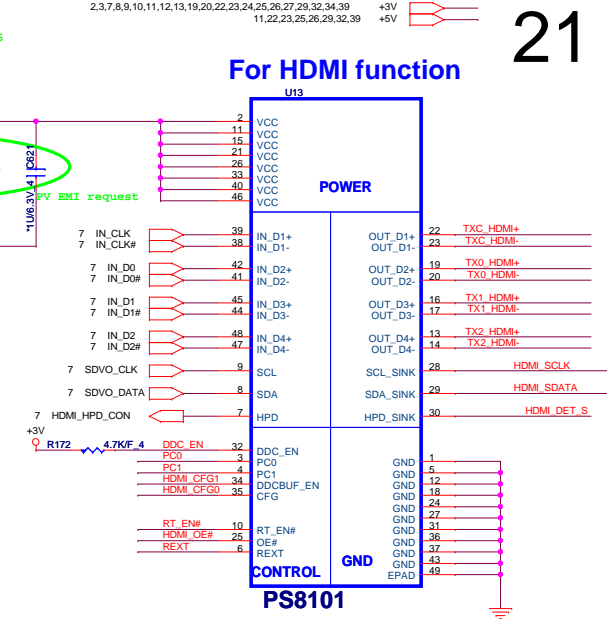
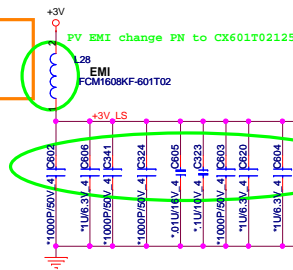
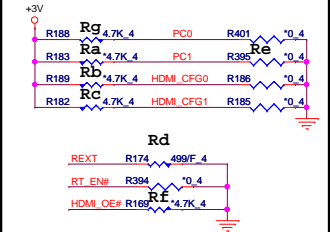
#### EQUALIZATION SETTING

PC1:PC0=0:0 8dB  
PC1:PC0=0:1 4dB Recommended  
PC1:PC0=1:0 12dB  
PC1:PC0=1:1 0dB

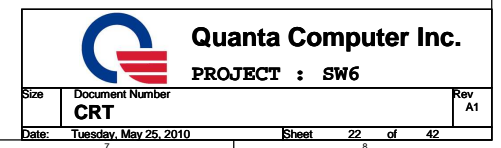
DDCBUF\_EN=1 DDC Active Buffer enable  
DDCBUF\_EN=0 DDC Passive Switch

SCLZ/SDAZ Low-level input/output Voltage  
CFG=0 VIL:<0.4V VOL:0.6V (Default)  
CFG=1 VIL:<0.44V VOL:0.66V

RT\_EN#:input 50ohm termination resistor enable internal PD  
OE#:TMDS output enable internal PD  
REXT :500 ohm to GND for analog current generation

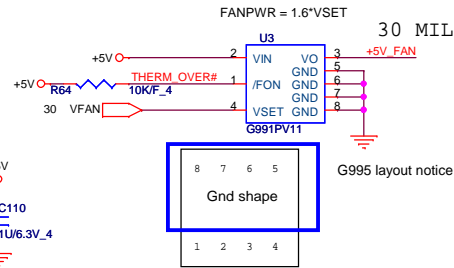
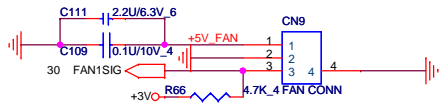




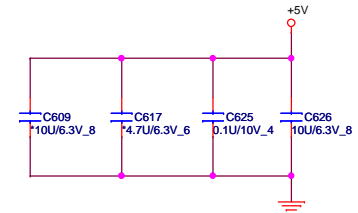
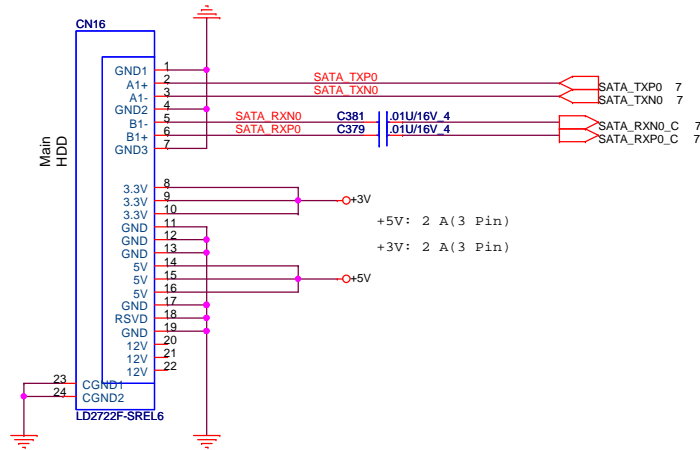




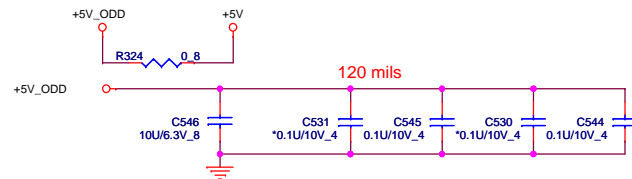
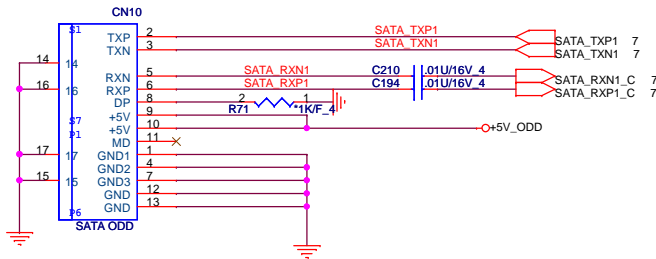
## CPU FAN



## SATA HDD CONNECTOR



## SATA ODD CONNECTOR

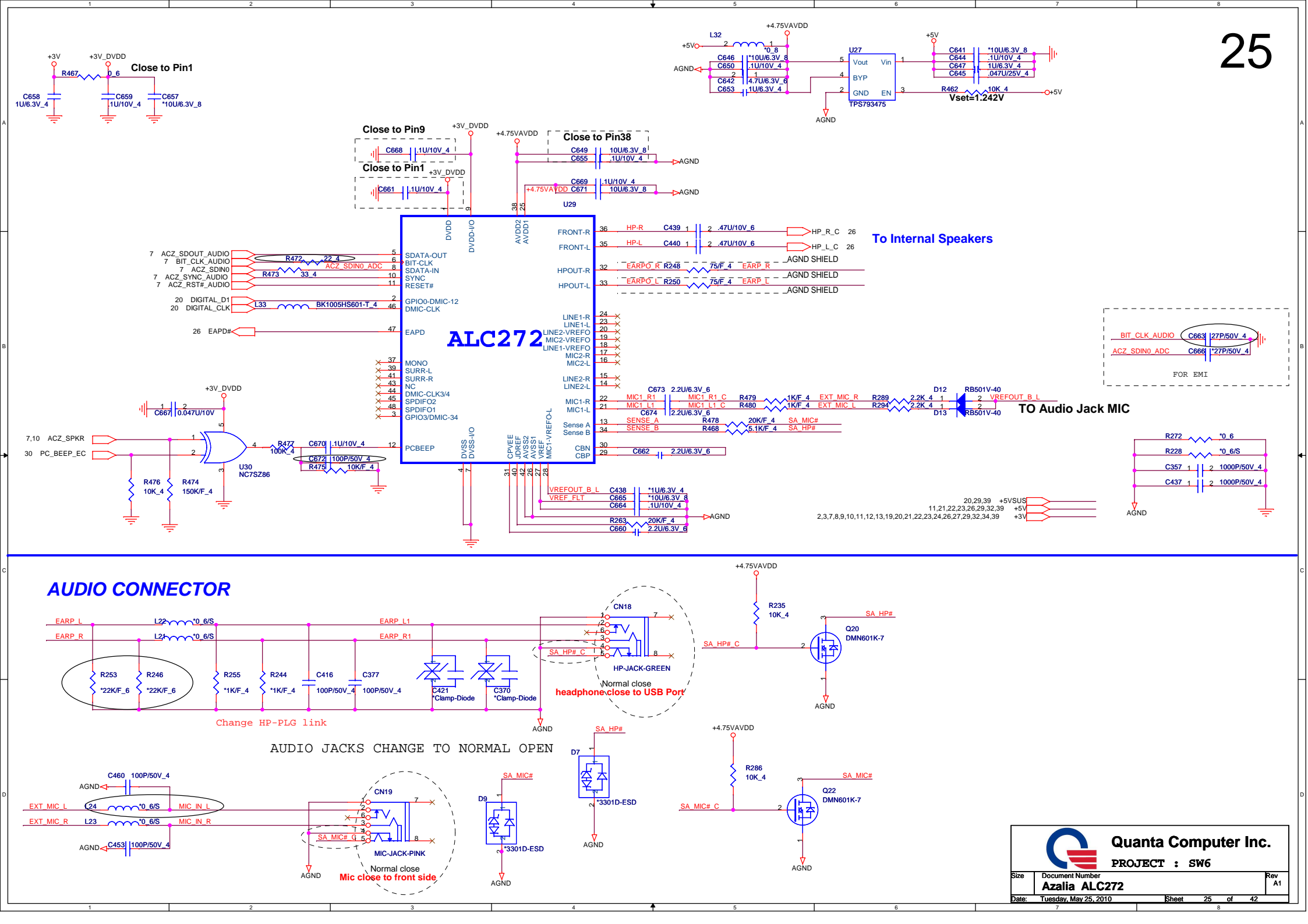


20,33,35,39 +15VALW  
11,21,22,25,26,29,32,39 +5V  
2,3,7,8,9,10,11,12,13,19,20,21,22,24,25,26,27,29,32,34,39 +3V



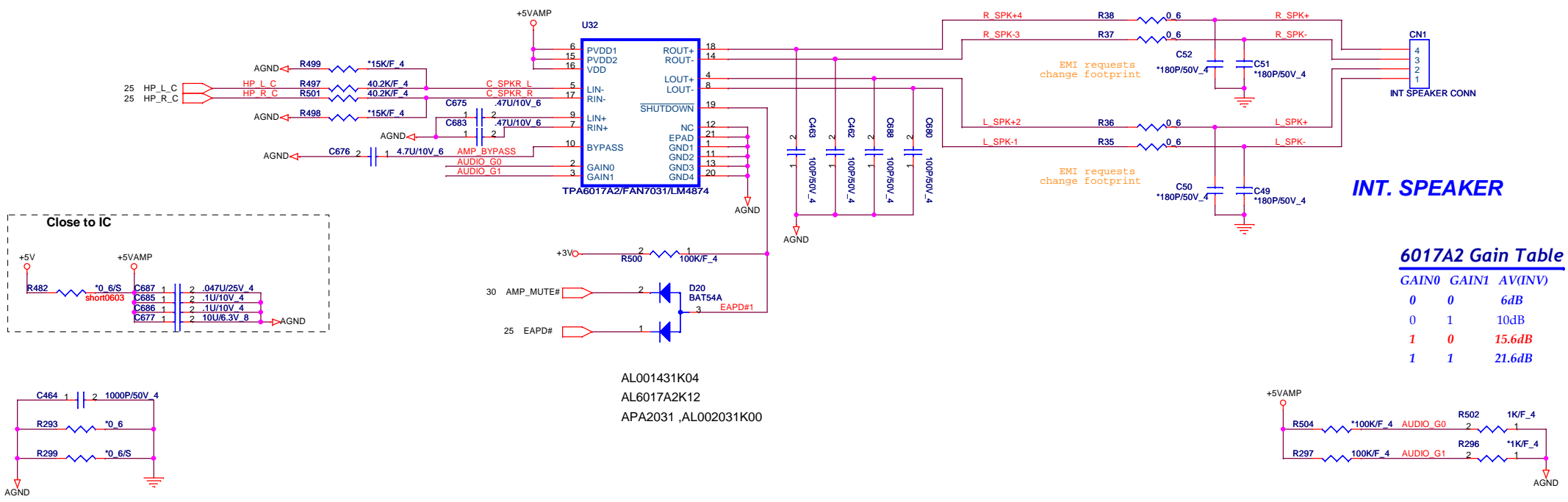




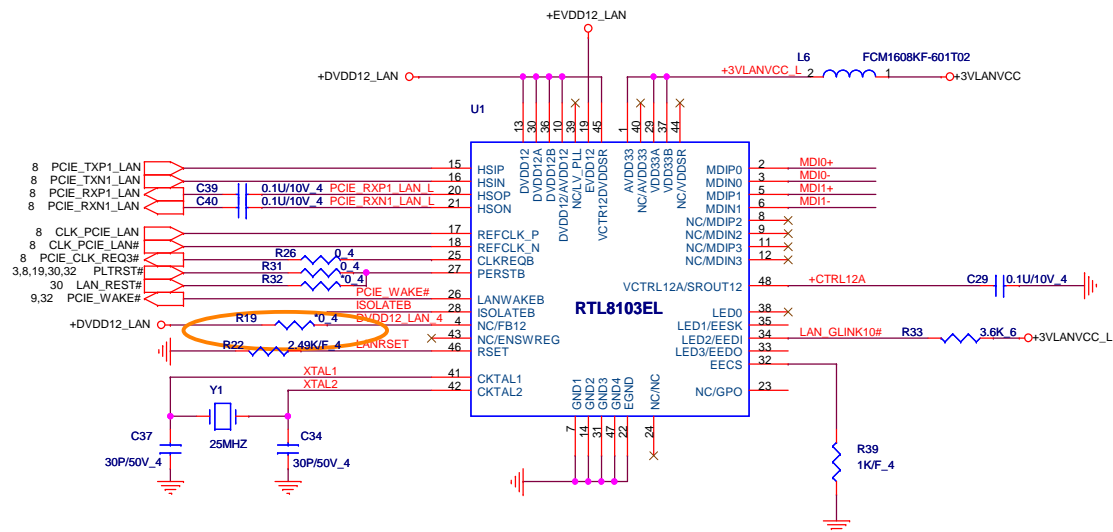




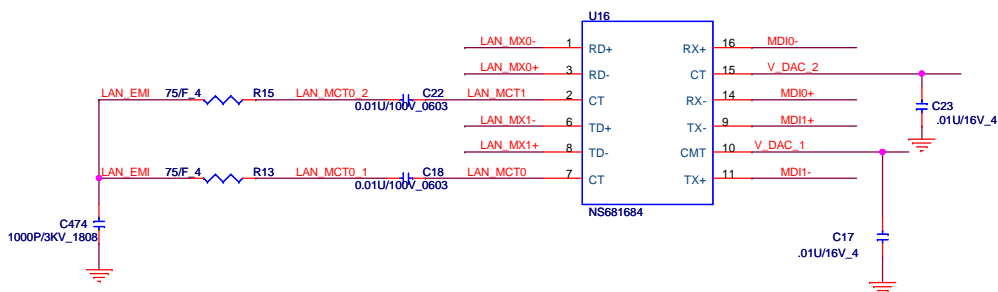
# AUDIO AMPLIFIER



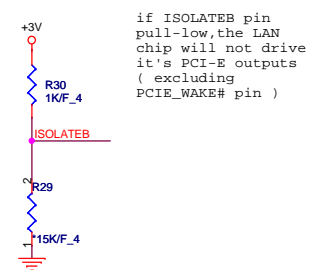
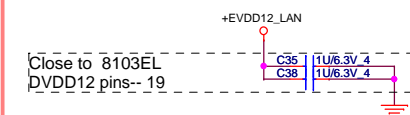
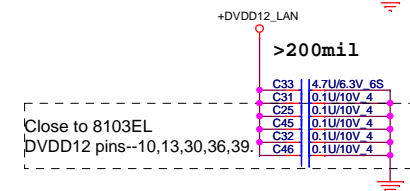
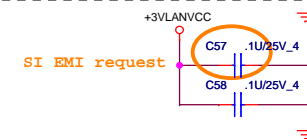
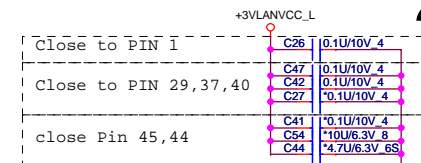
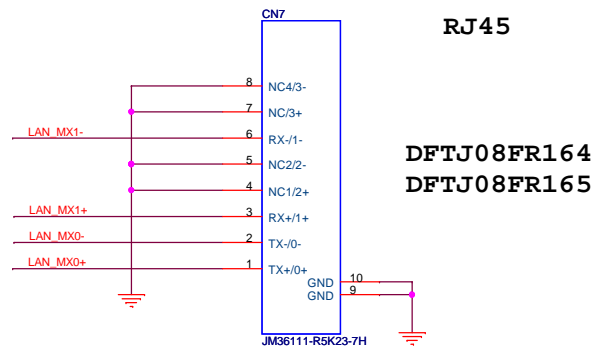
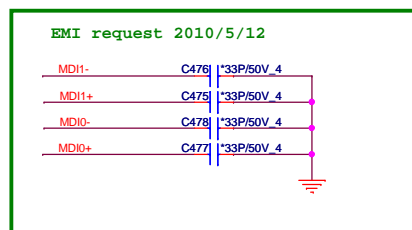




### Transformer for 10/100



### Lan Con.



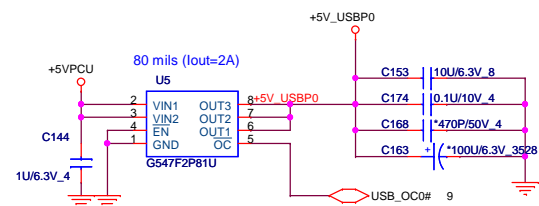
if ISOLATEB pin  
pull-low, the LAN  
chip will not drive  
it's PCI-E outputs  
( excluding  
PCIE\_WAKE# pin )

39 +3VLAVCC  
2,3,7,8,9,10,11,12,13,19,20,21,22,23,24,25,26,29,32,34,39 +3V



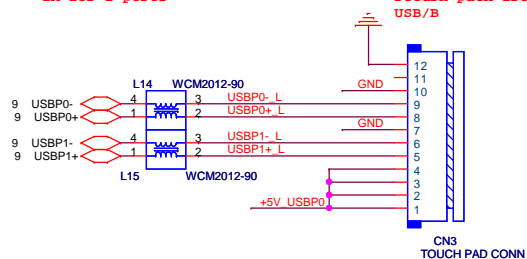
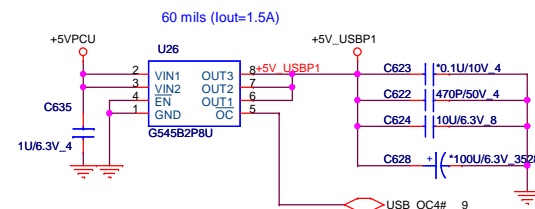
20,30,33,34,35,36,38,39,40,41

+5VPCU

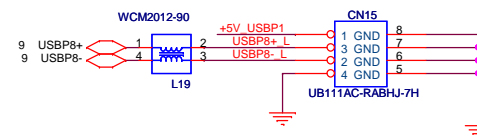
**Right SIDE USBX2**

USB I/O board Conn  
2A for 2 ports

PIN12 is for ESD  
return path from  
USB/B

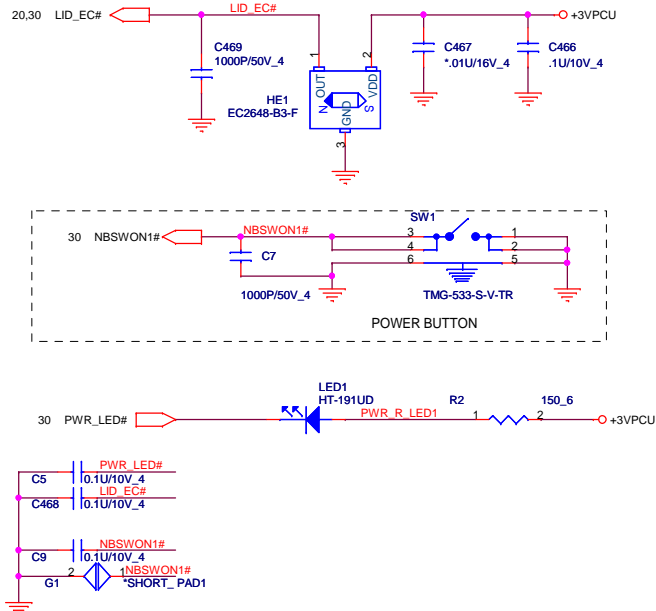
**LEFT SIDE USBX1**

1.5A

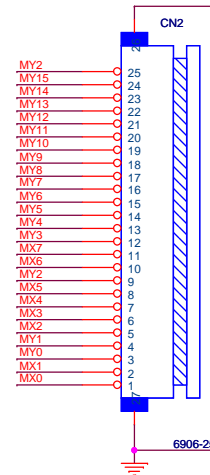
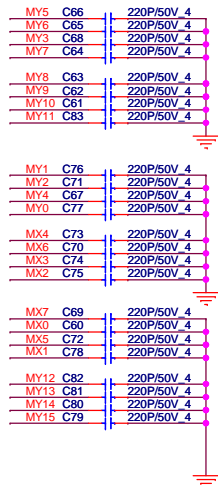




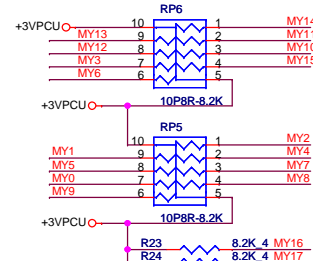
## POWER BOTTON CONNECT



## KEYBOARD Con.

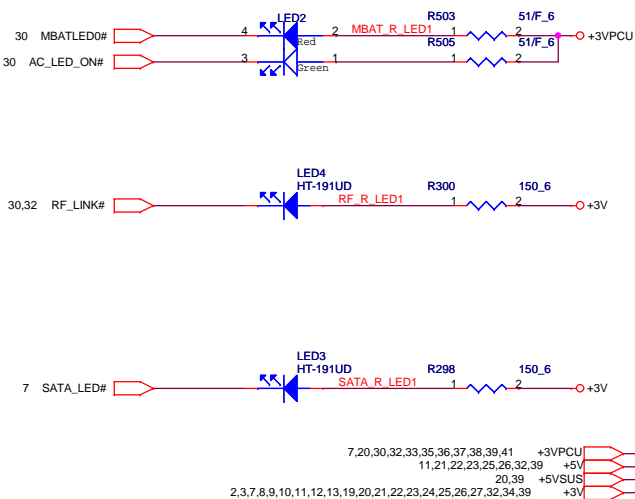


## KEYBOARD PULL-UP

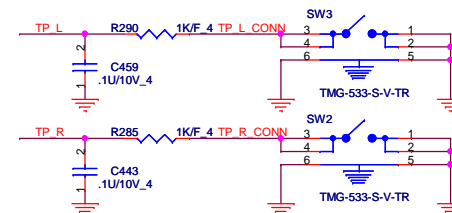
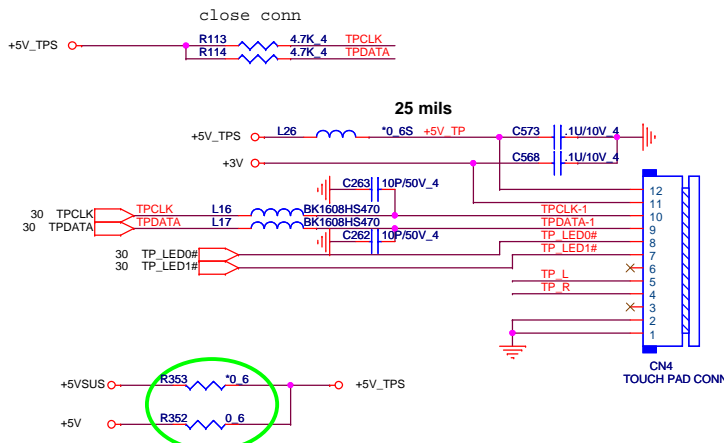


29

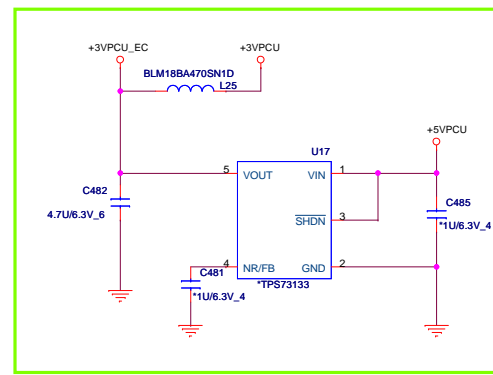
## TOUCH PAD Con.



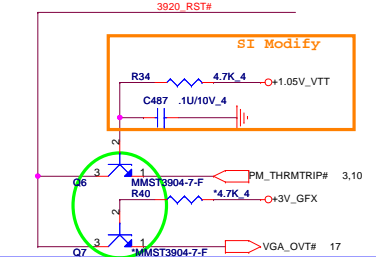
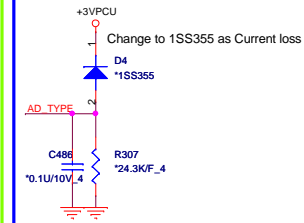
**TOUCH PAD SW**







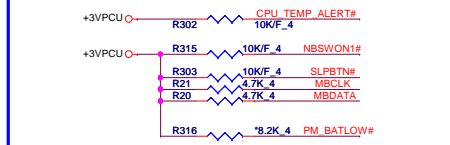
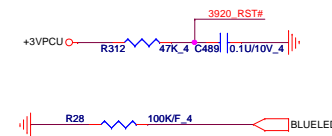
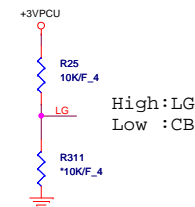
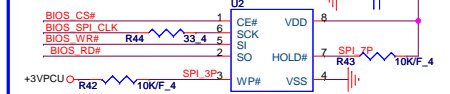
**thermal shutdown circuit**



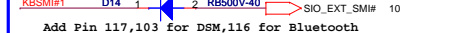
**512K byte SPI EC ROM**



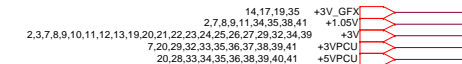
Socket: DG008000031  
MXIC AKE3KZP0001  
WINBOND AKE37ZN0N00  
AMIT AKE38ZN0800



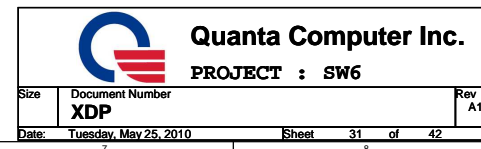
Change to RB500 as Current loss



Delete T10 and tie pin 117 from Lan for DSM

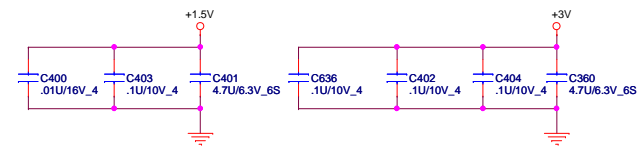
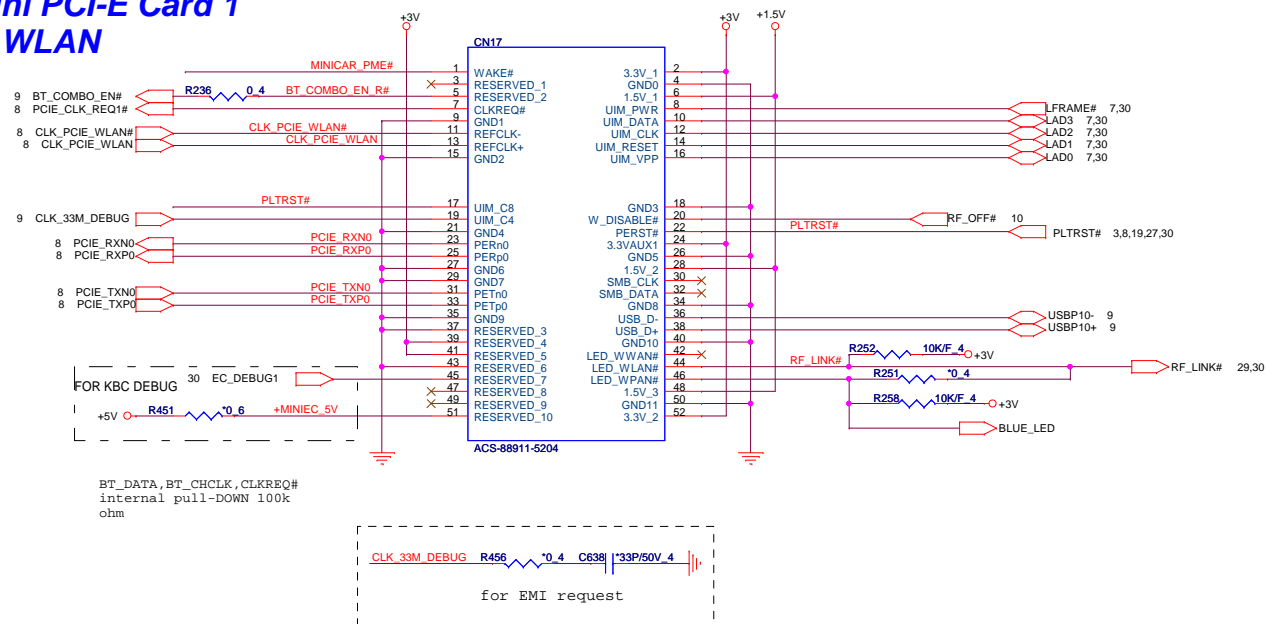




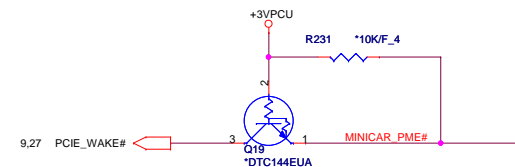




# Mini PCI-E Card 1 WLAN



INTEL WLAN  
CARD PIN 20  
W\_DISABLE#  
have  
internal  
pull-up 110k  
ohm



2,3,7,8,9,10,11,12,13,19,20,21,22,23,24,25,26,27,29,34,39 +1.5V  
7,20,29,30,33,35,36,37,38,39,41 +3V  
11,21,22,23,25,26,29,39 +5V

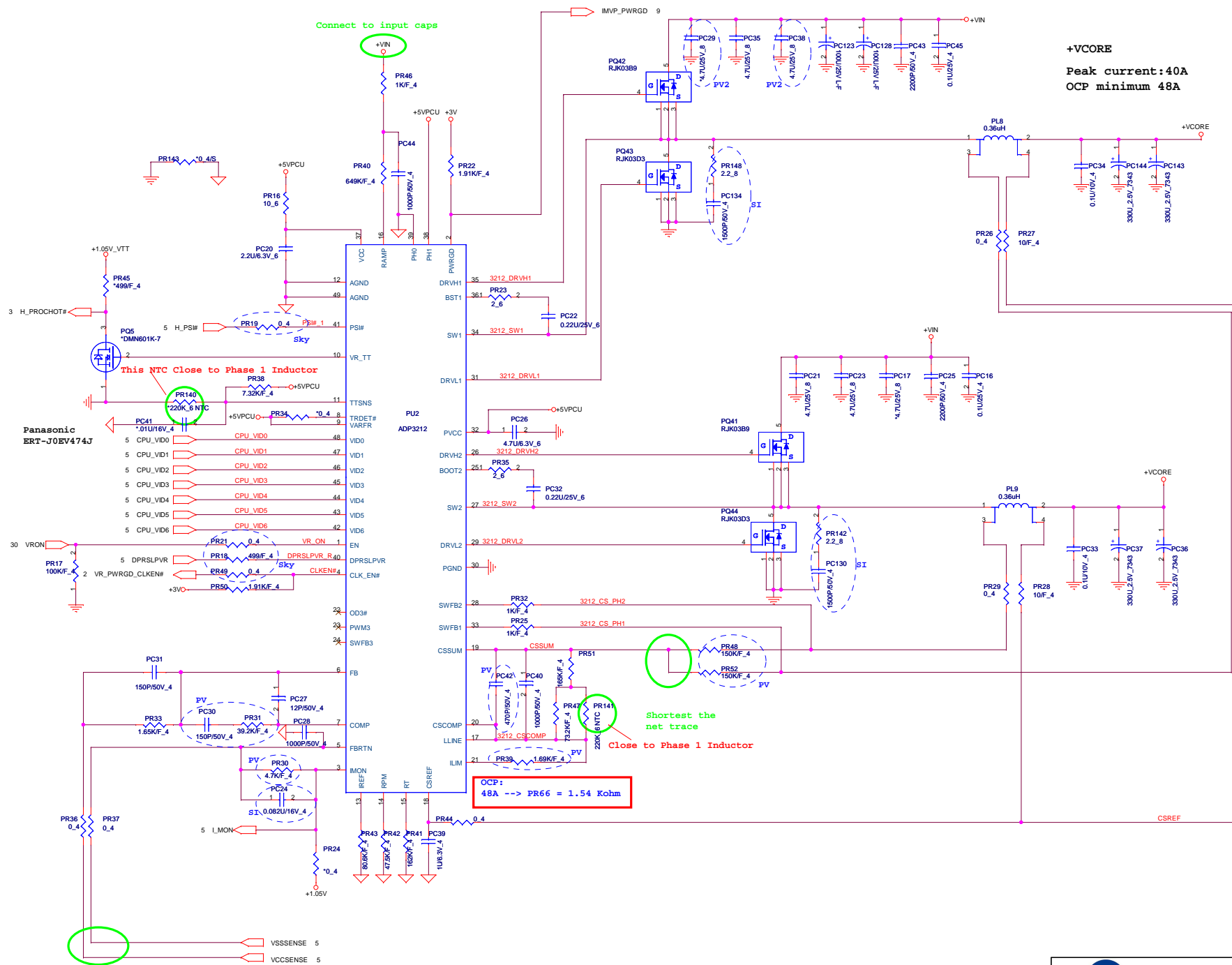
32





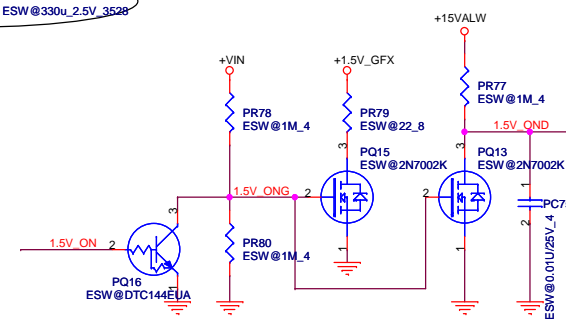
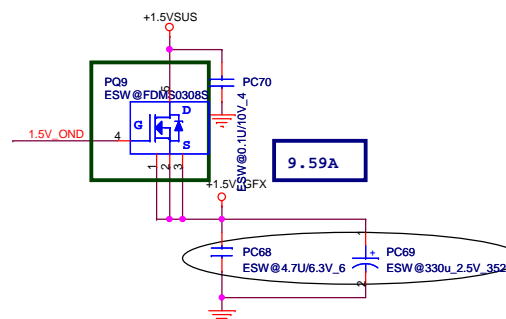
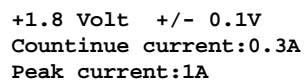
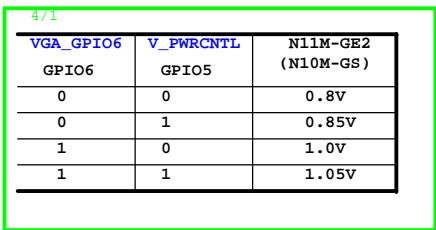


+VCORE  
Peak current:40A  
OCP minimum 48A

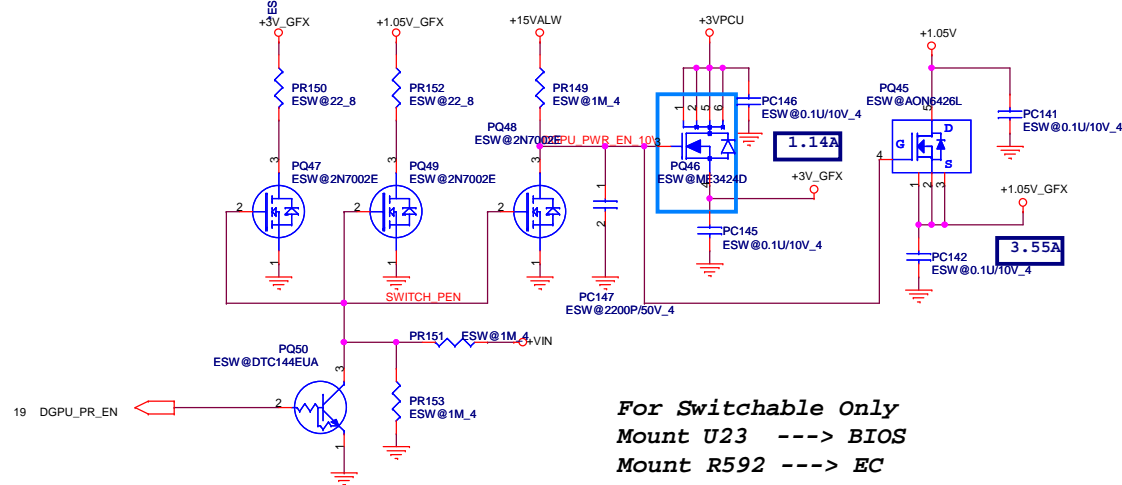




## 35



Change PC119 to 0.01u/25v as Discrete power sequence

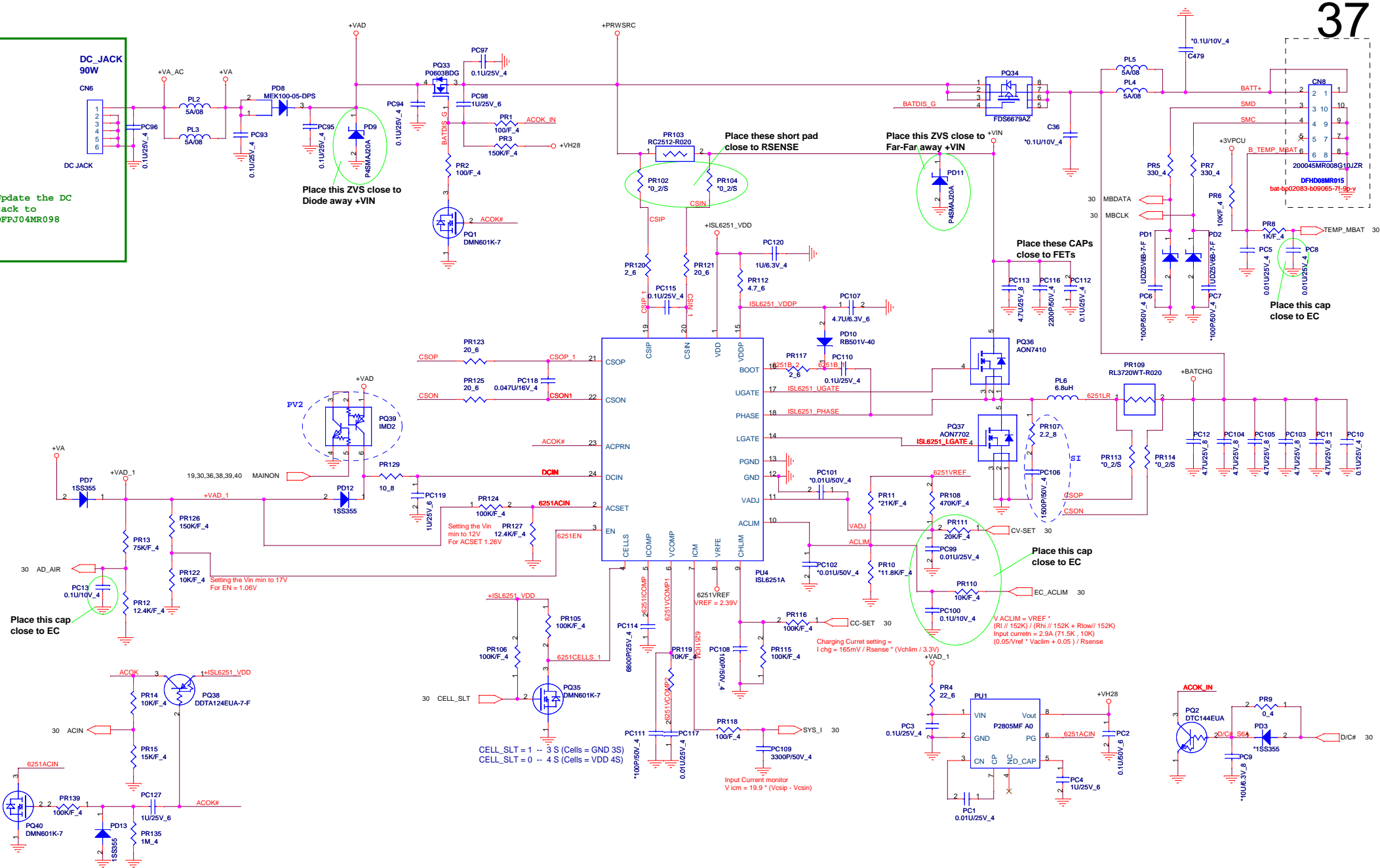


```
For Switchable Only
Mount U23 ---> BIOS
Mount R592 ---> EC
```

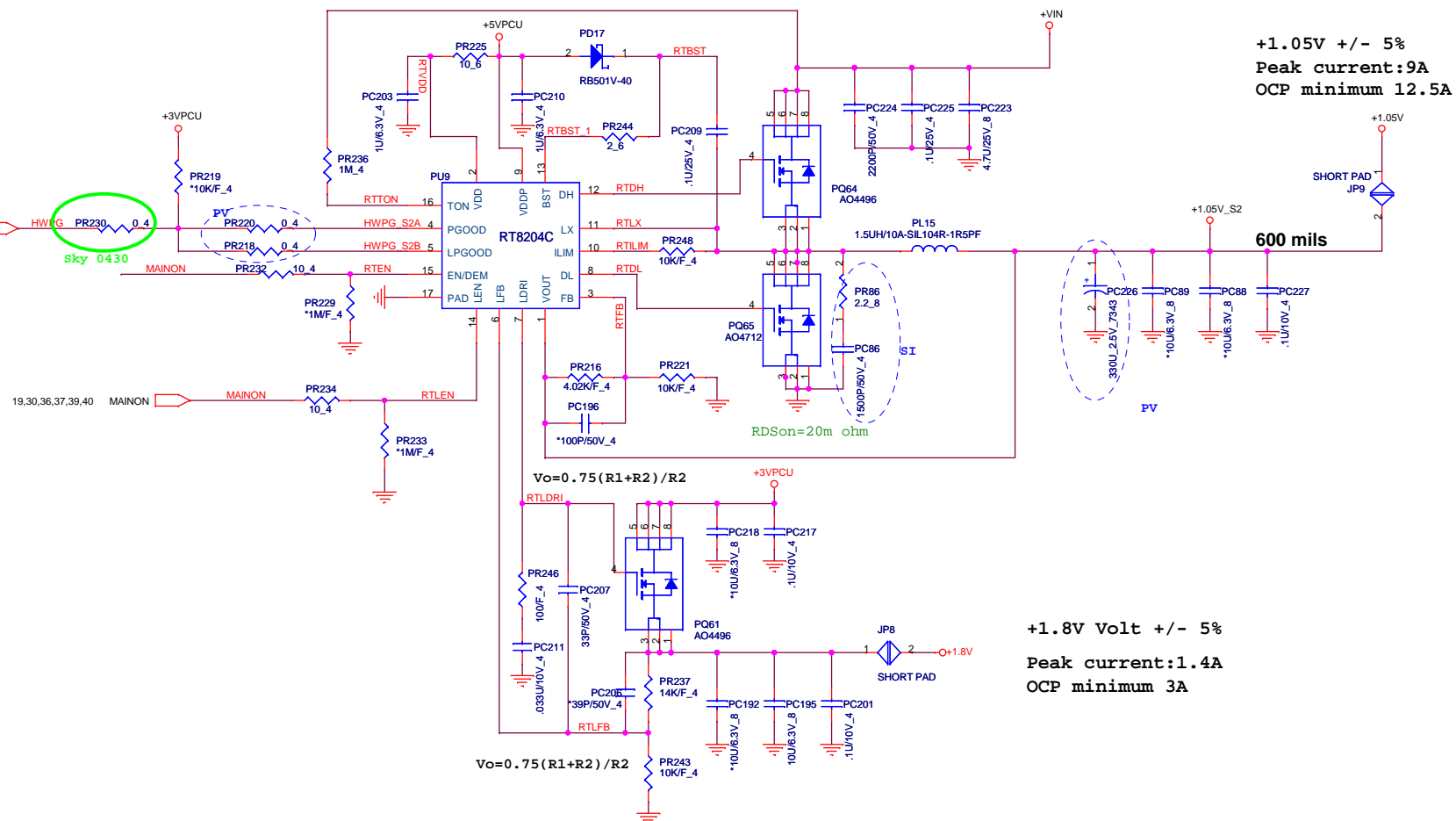




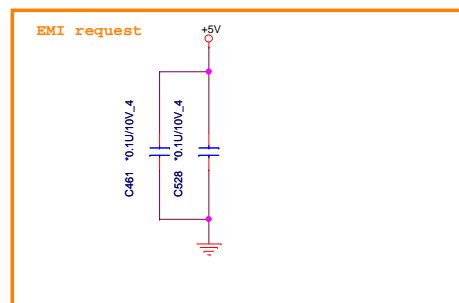
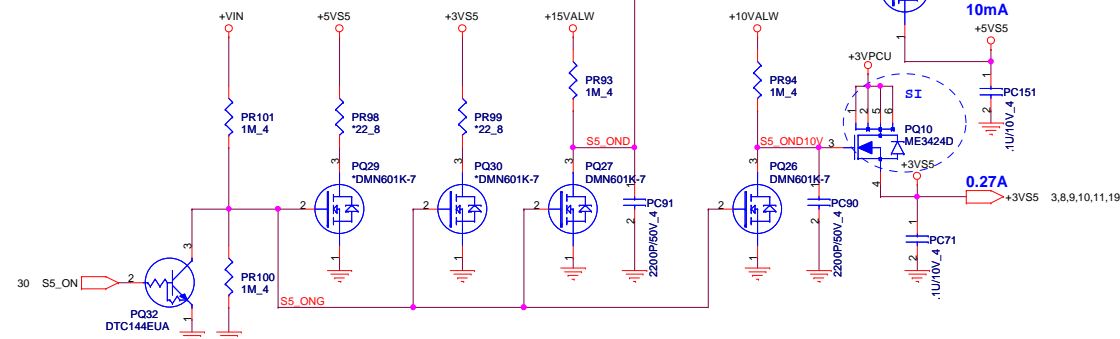
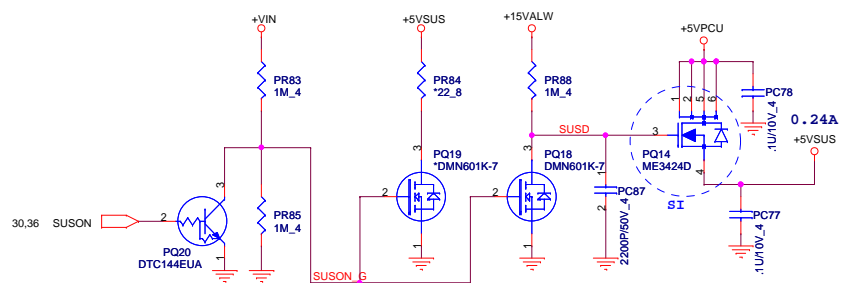
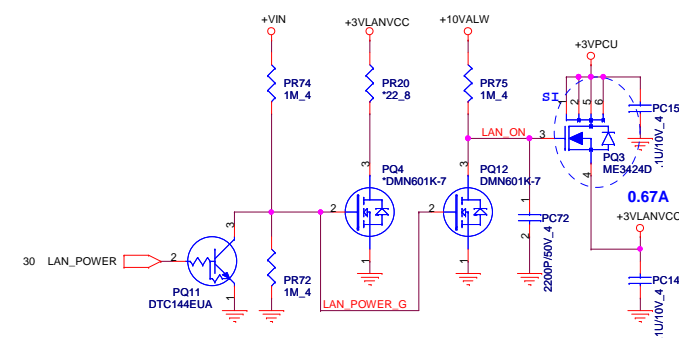
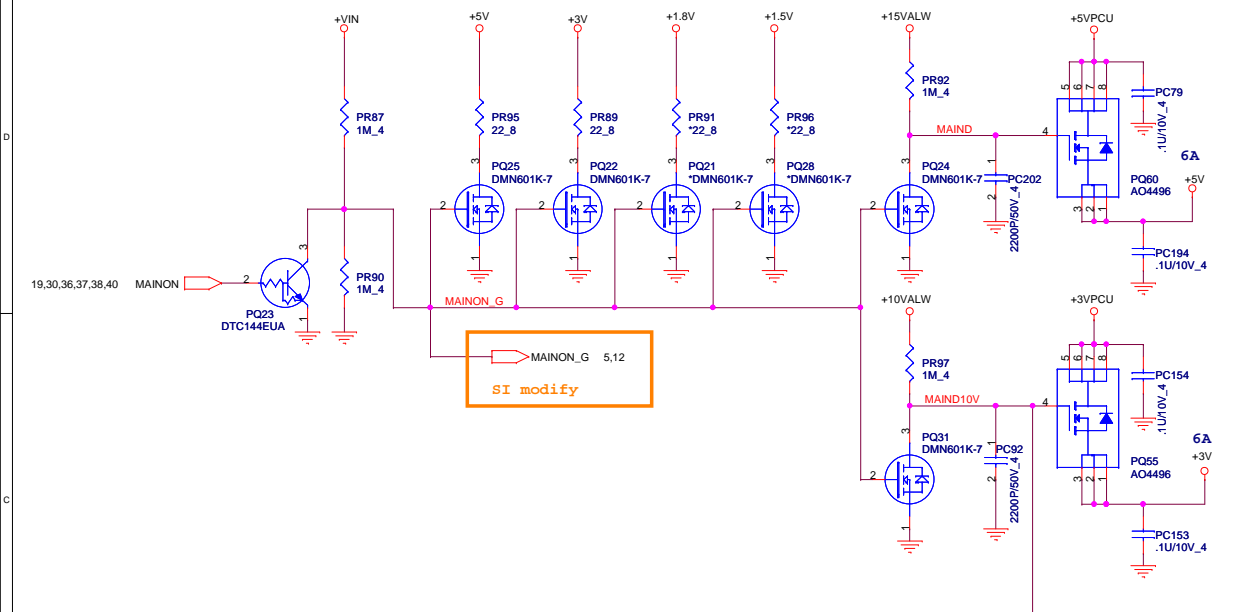




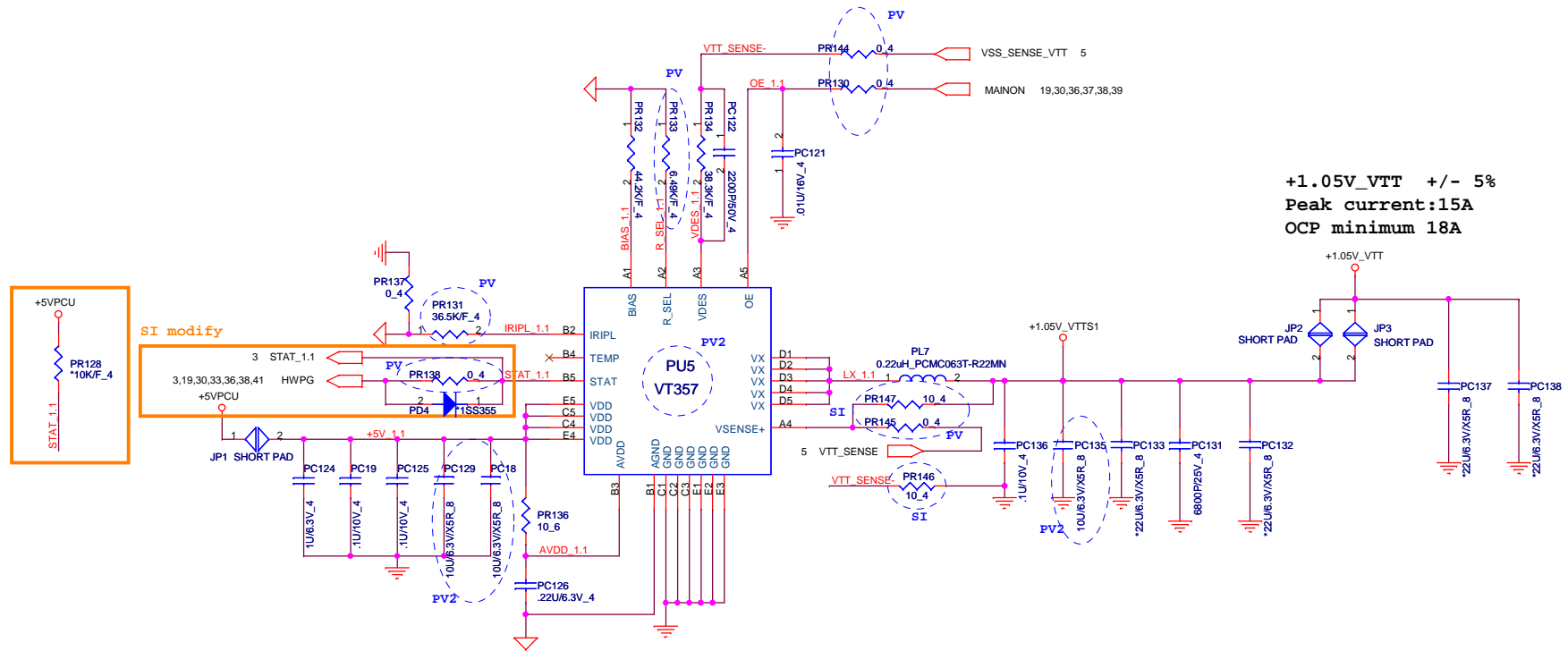










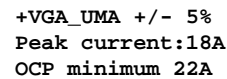


**Quanta Computer Inc.**

**PROJECT : SW6**

Size	Document Number	Rev
	<b>+1.05V_VTT (VT358)</b>	A1
Date:	Tuesday, May 25, 2010	Sheet 40 of 42







ITEM	DATE	PAGE	DESCRIPTION
1	5/8	2	AS EMI request, add C51 and C44 on page 2 for 27MHZ GPU CLOCK
2	5/8	24	AS EMI request, Change R538 from 0_S to 33ohm and move C786 to net SD_CLK and change value to 27p
3	5/8	27	AS EMI request, Add C580/C583/C585/C588 on the MDI interface
4	5/10	37	Modify the battery connector CN16 PCB footprint for DFHD08MR015
5	5/10	38	Change the PC237 from CC7390JMZ02 to be CH733RY8802 for height limited
6	5/10	35	Delete the JP11 and JP12 of VGA core
7	5/10	2	Update the Hole footprint and dimension
8	5/10	3	Change R179 from 0ohm short pad to 0ohm
9	5/11	28	Swap L28 and L31 pin connection for USB+/- trace routing
10	5/11	2	Add Hole16
11	5/11	41	Delete JP15 and JP16 for the power +VGACORE_IGPU
12	5/14	20	Delete U1,C18,R218,R18,R20,R17 and C13;Add D23,R350,C19,C22 and C390 for +3.6V_CAM
13	5/14	27	Swap LAN_MX1+/- with LANMX0+/-, and swap MDI0+/- and MID1+/- for EMI routing
14	5/14	28	Add R336 for the GND connection for M/B side and ESD side
15	5/14	2	Chagne hole18(H18) to AGND for Audio
16	5/18	29	Add LED5 and R355 for the WLAN+BT LED function
17	5/18	30	Delete Q17
18	5/18	32	Add R362 for Blue tooth LED funtion
19	5/18	20	Delete R19, Swap L4
20	5/18	2	Change H19,H5,H7 and H16 not connect to GND
21	5/18	19	Add R336 for the DGPU_PWR_EN function
22	5/18	28	Delete C344,C350,C426,C343 for Cost issue, Add C53 for +5V_USBP0, Change C46 from 0402 to 0805 type
23	5/20	2	Add Hole 22 for Fan module
24	5/20	27	Add R351 for U22.4 pin for DVDD12_LAN
25	5/21	28	Swap Pin defination for CN11
26	5/21	8/15	Change C10361 and C10437 from CH6102M9900(10u_0603) to CH61001ME96(10U_0805)
27	5/21	7	Delete C499 and C500 for LVDS clock signal
28	5/21	All	Back annotate from layout
29	5/24	13	Change R47 from 0_short to 0_0402
30	5/24	2	Update H2 to h-c256d118p2



